Verification of an IGBT Fusing Switch for Over-current Protection of the SNS HVCM

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***Abstract*-An IGBT based over-current protection system has been developed to detect faults and limit the damage caused by faults in high voltage converter modulators. During normal operation, an IGBT enables energy to be transferred from storage capacitors to a H-bridge. When a fault occurs, the over-current protection system detects the fault, limits the fault current and opens the IGBT to isolate the remaining stored energy from the fault. This paper presents an experimental verification of the over-current protection system under applicable conditions.**

Keywords-component; IGBT; modulator; high voltage; high current, protection, fuse

I. INTRODUCTION

The High Voltage Converter Modulators (HVCMs) at the Spallation Neutron Source (SNS) provide up to 11 MW pulses for various accelerator systems. The modulators employ resonant power conditioning techniques to generate up to 140 kV, 11 MW pulses from a ± 1.2 kV, 0.2 MJ capacitor bank [1].

Several fault mechanisms that result in a destructive release of energy from the capacitor bank to other regions of the modulator have been observed. These include IGBT failures, attributed to thermal cycling, shoot through, or transformer saturation [2], and arcing or tracking between high voltage components on or after the H-bridge. There are ongoing improvement programs to reduce modulator susceptibility to these faults [3, 4].

Under collaboration between SNS and the SLAC National Accelerator Laboratory, an IGBT fusing switch and gate drive system is under development to protect the HVCM during a fault [2, 5, 6, 7]. A normally conducting IGBT fusing switch is to be added between the energy storage bank and the H-bridge. When a fault is detected, the fusing switch will isolate the stored energy from the fault. Without a fuse to open during a fault, the peak fault current will reach unacceptable amounts. With a normal self destructive fuse, over current protection exists but must be but will necessitate maintenance after a fault. By using an IGBT, the gate voltage will limit the peak fault current prior to turning off, turn off in a controlled manner and maintain the ability to turn back on once the fault is cleared.

Desaturation of the fusing switch is used limit the maximum fault current. On detection of a fault, the fusing switch will open. Two detection mechanisms are used to identify a fault condition. A $V_{ce,sat}$ monitor in the gate drive circuitry detects excess peak current through the fusing IGBT. Additionally, excessive rate of rise in the current through the fusing IGBT is detected with an L·di/dt monitor.

The design of the fusing switch protection system was presented in [5]. A test stand was constructed to experimentally characterize the fusing switch and determine the optimum gate drive parameters. The results of this characterization are presented in this paper. We found that without taking precautions to stabilize the gate-emitter voltage during a fault, the peak current rose to an unacceptable magnitude before the fusing switch could turn off. But by stabilizing the gate voltage with a large gate-emitter capacitance added directly to the IGBT fusing switch, rather than at the gate drive circuitry, the peak current was limited by IGBT de-saturation and the fusing switch was able to turn off and isolate the stored energy in an appropriate amount of time.

II. PROTECTION SYSTEM DESCRIPTION

In order to safely isolate the stored energy in the capacitor bank during a fault, the fusing switch must be arranged in between and in series with the capacitor bank and the H-bridge of the SNS modulator. Normal operation of the fusing switch means that the switch is *on* and is either conducting or ready to conduct current depending on the state of the modulator. Only after a fault has been detected will the fusing switches open. In this configuration, all nodes of the IGBT are at approximately the same potential as the storage capacitors. This arrangement requires the IGBT driving circuit to employ high voltage isolation such that the driving circuit is common to the emitter of the IGBT. Fig. *1* shows the location of the fusing switches in the HVCM circuit. The switches are not in parallel, and therefore, current sharing schemes are not necessary.

Due to the high voltage bias of the driver circuit, communication between the modulator control system and the fusing switch gate drive is made via optically isolated signals. If a fault occurs, the gate drive will detect the fault and lower the IGBT gate voltage. Once a fault is detected, a second optical fault signal is routed to ground potential so that the fault can be logged and other actions can be enacted.

The gate drive can provide 11 – 16 V to the IGBT fusing switch gate-emitter terminal. During normal operation, a low

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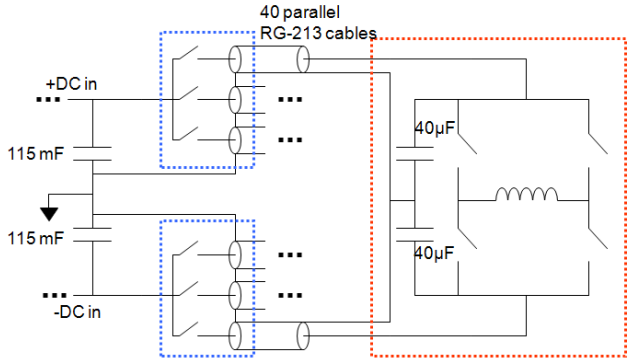

Fig. 1: Simple circuit diagram of the placement of the fusing switches (highlighted in blue). Only one (highlighted in red) of three H-bridges is shown. The capacitors at the left represent the 180 kJ capacitor bank.

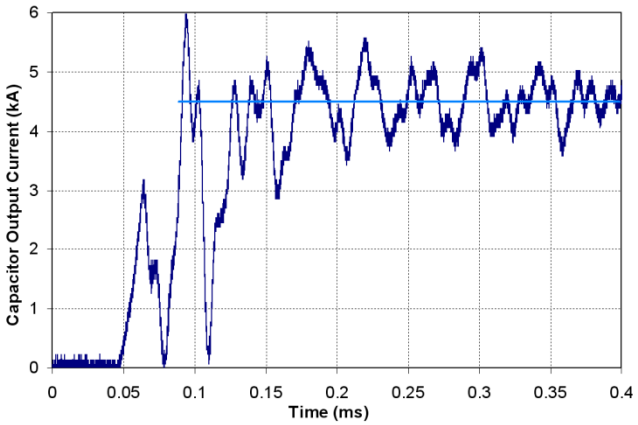

Fig. 2: Measured SNS HVCM current from the capacitor bank to the H-bridges. Shown is the start of the pulse.

gate drive voltage will lead to higher conduction losses of the IGBT. During a fault, a high gate voltage will lead to high peak fault current as the fusing switch leaves saturation. A gate voltage of 15 V was determined to provide adequate control of fault current while keeping normal conduction losses within an acceptable limit.

A fault is detected by the gate drive circuit by measuring the collector emitter saturation voltage, $V_{CE,SAT}$, while the fusing switch is conducting. During a fault, there is a rapid increase in collector current, which corresponds to a measurable increase in $V_{CE,SAT}$. Once $V_{CE,SAT}$ has surpassed a predetermined value, 13 V, the gate drive turns the fusing switch *off*. The peak fault current is determined by the transfer characteristics of the IGBT.

Fig. 2 shows the measured current through the existing high-energy capacitor banks of the SNS HVCM. The current is split evenly between each of the three H-bridges. Therefore, each fusing switch would be expected to conduct ~1.5 kA during the pulse. The IGBT selected for use as a fusing switch was the Eupec FZ800R33KL2C [8]. This module has a blocking voltage of 3.3 kV and a repetitive peak current rating of 1.6 kA. From the transfer curves on the IGBT data sheet, with a conduction current of 1.5 kA and a gate-emitter voltage of 15 V, the collector-emitter voltage drop is ~5.5V. At full HVCM average power, the estimated conduction power losses per IGBT are

$$(5.5V_{CE})(1.5kA)(60Hz)(1.6ms) \approx 800W \quad (1)$$

The total FS power consumption for the six fusing switches is 4.8 kW. For a 1 MW average power modulator, this is 0.5% of the total power output.

A cooling water distribution system already exists on each HVCM. Because there is limited space around the capacitor buses, water cooling was chosen for heat management for the IGBTs. A commercial off the shelf, 4-pass liquid cold plate was chosen. With 800 W power dissipation per device, the junction temperature of each IGBT is calculated to be ~70 °C.

III. Experiment

A. Setup

The fusing switch system was tested in a test stand that mimicked normal operation in the SNS HVCM. An energy storage capacitor was charged to high voltage, 1 – 2 kV. The fusing switch was then closed which allowed current to flow through the fusing switch and the load resistor. Once normal conduction was established, a trigatron spark gap was used to simulate a fault condition by shorting out the load resistance.

Fig. 3 depicts the circuit used to test the fusing switch. As current quickly rose through the fault, the fusing switch was used to limit the current by coming out of saturation. Simultaneously the gate drive detected the fault and turned off the fusing switch in a controlled manner. A variable inductance was inserted between the fusing switch and the load resistance to sweep di/dt for a given charge voltage. The minimum total circuit inductance was measured at 98 nH.

Tests were performed to explore the fault characteristics of the IGBT including any effects of the Miller capacitance in determining current during a fault. Factors of interest for the gate drive included V_{GE}, and C_{GE}. The inductance in series with the switch was varied to determine its effect. Response variables of interest included peak current and di/dt at fault, and the ability to retain control of the device via the gate.

B. Data

Fig. 4 displays the fusing switch collector current before, during, and after a fault. For 15 μs, the fusing switch was closed and current flowed through the load resistance. At about 15 μs, the fault was initiated and current quickly increased. During initial tests, the peak fault current rose as high as 10 kA. The charge voltage and the total circuit inductance determined di/dt during the fault. By decreasing the gate voltage the peak current was only slightly reduced, indicating that the gate voltage was doing little to control the peak current.

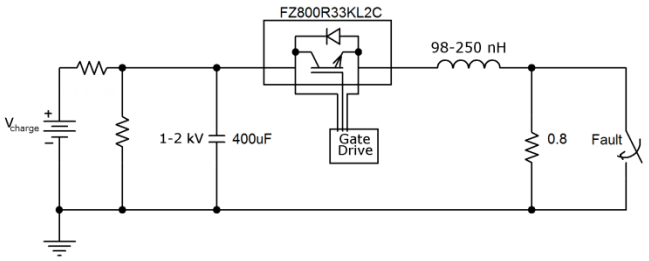

Fig. 3: The fusing switch test circuit.

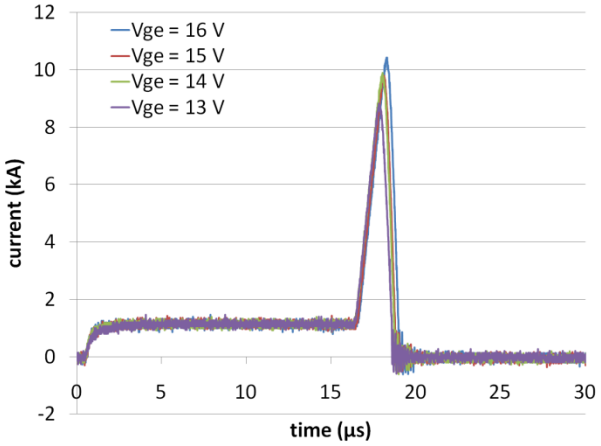

Fig. 4: Fusing switch collector current measured with the test circuit before, during and after a fault. The gate voltage was varied to determine the ability of the switch to limit current via desaturation.

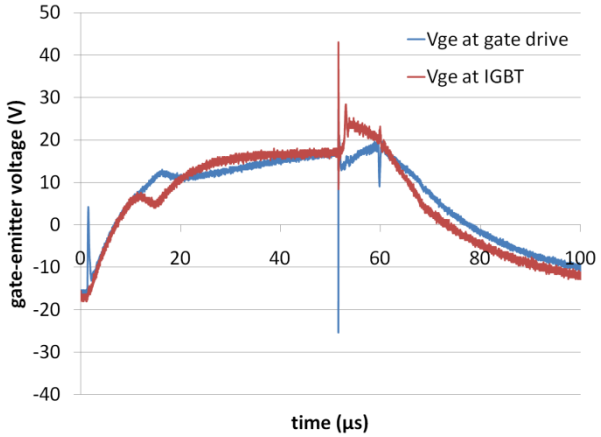

Fig. 5: A difference in gate-emitter voltage was observed between the gate drive circuit and directly at the IGBT.

Fig. 5 compares the gate voltage measured directly at the gate drive circuit to the gate voltage measured directly at the IGBT. A discrepancy between the voltages was observed. V_{GE} measured directly at the IGBT jumped from 15 V to 25 V during the fault indicating that Miller capacitance was driving the gate voltage higher. It was determined that Miller capacitance combined with impedance between the gate driver and IGBT leads to reduced gate control.

To counteract the effects of the Miller capacitance and to ensure that V_{GE} was stabilized at the IGBT rather than only at the gate driver, large capacitance was added between the gate

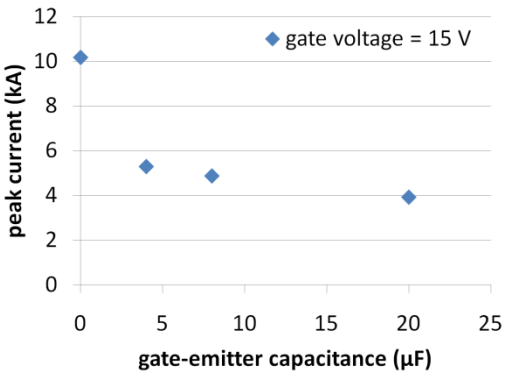

Fig. 6: By increasing the gate-emitter capacitance directly at the IGBT, the peak fault current was reduced.

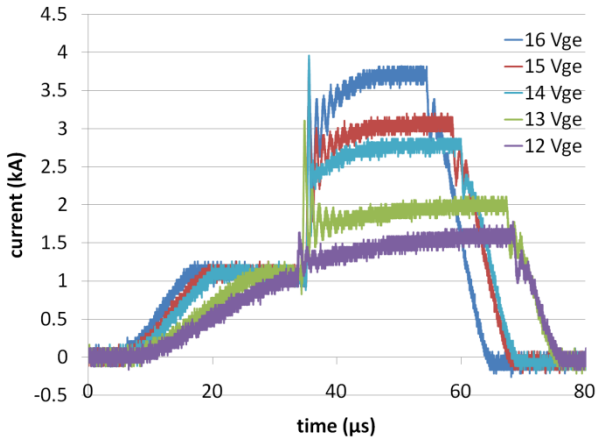

Fig. 7: After gate-emitter capacitance was added, the peak fault current was observed to plateau when the fusing switch exited saturation. These data were taken with 20 µF C_{GE}.

and emitter directly at the IGBT. By increasing the gate-emitter capacitance from around 200 nF to as high as 20 µF, the impedance between the gate driver and the IGBT was circumvented from playing a role in destabilizing the gate voltage. The data in Fig. 6 show that as a result, the peak current during a fault was dramatically reduced.

By reestablishing control of the gate-emitter voltage, the fusing switch was observed to exit saturation and control the fault current during a fault. A higher level of control is attainable by reducing the fusing switch gate voltage. Once gate control was reestablished, the fault current was observed to plateau as shown in Fig. 7. Because a small, but finite impedance exists between the exterior of the IGBT module and the module's interior devices, a small but limited current spike still occurs before control of the IGBT is regained.

While peak current was limited, the 20 µF gate-emitter capacitance also increased the turn on, and turn off time of the fusing switch by ~ 20 µs. However, because the fusing switch is normally on, a long turn on time does not adversely affect the performance of the switch. In addition, an increased turn off time meant that dv/dt feedback through the gate-collector capacitance was unlikely to turn the IGBT back on.

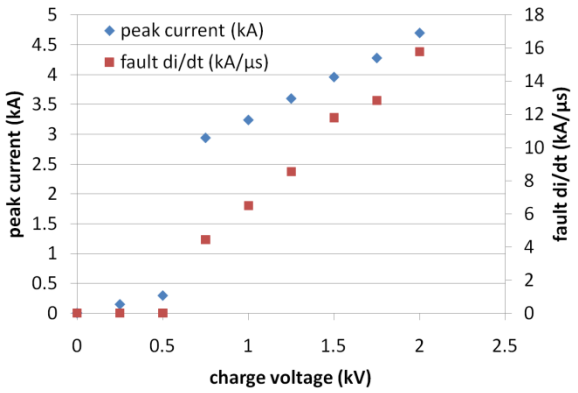

Fig. 8: The fusing switch was successful in conrolling the fault current over a wide range of di/dt. This was tested by changing the capacitor charge voltage.

Fig. 7, shows the fault current after a 20 µF capacitance was added between gate and emitter. By comparing Fig. *4* and Fig. *7*, it is apparent that the total fault conduction time increased with the added gate-emitter capacitance. This is because $V_{CE(SAT)}$ takes longer to rise with a lower fault current. Because the magnitude of the fault current is limited, the longer conduction time is acceptable. A relatively small amount of energy, 250 J, is transferred through the fusing switch to the fault before the fusing switch fully opens.

In the SNS circuit, the location of a fault will dictate the fault circuit inductance and thus di/dt during a fault. To ensure the fusing switch would operate under all di/dt conditions, the charge voltage of the test circuit storage capacitors was varied and the circuit inductance was minimized. By increasing the charge voltage, di/dt was increased according to

$$\frac{di}{dt} = \frac{V_{cap} - V_{CE}}{L_{circuit}} . \qquad (2)$$

As the charge voltage approached 2 kV, di/dt approached the anticipated worst case scenario for the SNS HVCM. Fig. 8 displays the peak current and the fault di/dt for this experiment. The fusing switch was operated with a gate voltage of 15 V and a 20 µF gate – emitter capacitor. The fusing switch was successful in suppressing the fault current and isolating the stored energy with di/dt as high as 15.7 kA/µs.

IV. Summary

Experimentation has been performed to validate the operation of the IGBT fusing switch and accompanying gate driver. We found that without a large stabilizing gate-emitter capacitance, the fusing switch could be turned off after detecting a fault but would not limit peak current to an appropriate level by desaturation. By increasing the gate emitter-capacitance to a large value, 20 µF, and by mounting the gate-emitter capacitance directly to the IGBT fusing switch, peak current was limited to an acceptable level.

The added gate-emitter capacitance increased turn on and turn off time. However, because the fusing switch is normally on, and because the added capacitance encouraged desaturation to limit peak fault current, a fast fusing switch turn off time was not necessary.

The fusing switch was tested in a test stand that mimicked fault conditions in the SNS HVCM. The protection system was found to detect, appropriately control, and isolate stored energy after the fault. The system was found to perform well with an on-state gate voltage of 15 V so that normal conduction losses would within acceptable amounts.

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