SLAC-PUB-15640

ePix: a class of architectures for second generation LCLS cameras

A Dragone, P Caragiulo, B Markovic, R Herbst, B Reese, S C Herrmann, P A Hart, J Segal, G A Carini, C J Kenney and G Haller

SLAC National Accelerator Laboratory, 2575 Sand Hill Rd., Menlo Park, CA, USA

E-mail: dragone@slac.stanford.edu

Abstract. ePix is a novel class of ASIC architectures, based on a common platform, optimized to build modular scalable detectors for LCLS. The platform architecture is composed of a random access analog matrix of pixel with global shutter, fast parallel column readout, and dedicated sigma-delta analog-to-digital converters per column. It also implements a dedicated control interface and all the required support electronics to perform configuration, calibration and readout of the matrix. Based on this platform a class of front-end ASICs and several camera modules, meeting different requirements, can be developed by designing specific pixel architectures. This approach reduces development time and expands the possibility of integration of detector modules with different size, shape or functionality in the same camera. The ePix platform is currently under development together with the first two integrating pixel architectures: ePix100 dedicated to ultra low noise applications and ePix10k for high dynamic range applications.

1. Introduction

The unique characteristics of Free-Electron Laser (FEL) sources in terms of brilliance and narrow pulse duration have increased the need of new large area detectors with fast readout and specifications that, depending on the experiment, can range from ultra low noise requirements [1] to extremely large full-scale and dynamic ranges [2]. The first years of the Linac Coherent Light Source (LCLS) operation have shown the need to support a wide variety of experiments with a correspondent variety of detectors with different shapes, areas and functionalities. The harsh nature of FEL sources also increases the risks of damages during operation and parts of the cameras need to be replaced often which has an impact on cost. Modular scalable detectors with standardized interfaces and communication protocols are key factors to provide time and cost effective cameras, easy to adapt and support. Only integrating detectors can be used in FEL applications and those based on architectures with a higher level of parallelism has proven to be more suitable. Hybrid pixel detectors seem at the moment the best compromise between performance and complexity [3]. Several configurations are possible within a hybrid approach and an optimal level of parallelism needs to be determined. ePix is a novel class of ASICs integrating architectures based on a common platform optimized for processing the signals from LCLS cameras. This platform is composed of a random access analog matrix of pixels with global shutter, fast parallel column readout, and dedicated sigma-delta analog-to-digital converters per column. It also implements a dedicated control interface and all the required support electronics to perform configuration, calibration and readout of the matrix. The ePix development has

Presented at the 17th Pan-American Synchrotron Radiation Instrumentation Conference
Gaithersburg, MD, USA, June 19 - 21, 2013

Work supported by US Department of Energy contract DE-AC02-76SF00515 and BES.

been scheduled in phases. Each phase will produce a device with sufficient functionality to be used in scientific experiments. Subsequent phases will incrementally increase area and speed of the device.
Based on this platform a class of front-end ASICs and several camera modules, meeting different requirements, can be developed using different pixel architecture variants. This approach reduces development time and expands the possibility of integration of detector modules with different size, shape or functionality assembled in the same camera.
The ePix platform is currently under development together with two integrating pixel variants (table 1): ePix100, optimized for ultra low noise applications with resolution of less than 100e^- r.m.s. and a signal range of 35fC (100 photons at 8keV), and ePix10k, optimized for high dynamic range applications with resolution of less than 350e^- r.m.s. and a signal range of 3.5pC (10k photons at 8keV). The first prototype versions of the ASICs are fabricated in TSMC CMOS 0.25µm technology.

2. ePix platform architecture

The ePix platform architecture (figure 1) is composed of an analog matrix of pixel with global shutter, fast parallel column readout, and dedicated sigma-delta analog-to-digital converters per column.

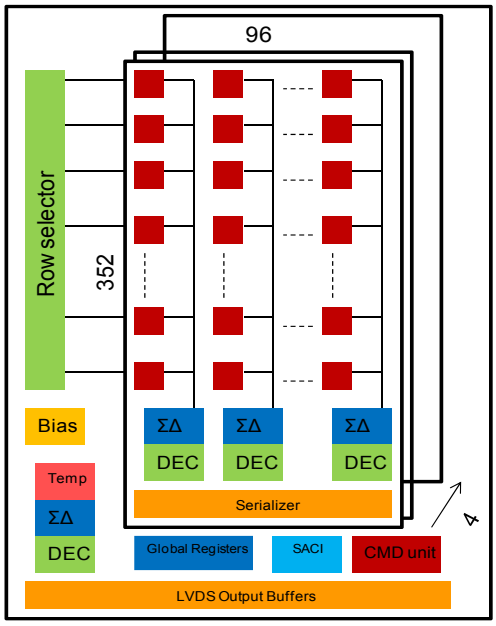

Figure 1. Simplified block diagram of the ePix Platform (number of rows and column reported are for ePix100).

Table 1. ePix ASICs characteristics

	ePix100	ePix10k
Pixel size	50x50 µm^2	100x100 µm^2
Array size	352x384	176x192
Frame rate	500Hz (min. req. 120Hz)	1kHz (min. req. 120Hz)
Signal range	220ke$^-$	22Me$^-$
ENC	50e$^-$ (min. req. 100e$^-$)	120e$^-$ (min. req. 350e$^-$)
Gains	6.5µV/e$^-$	6.5µV/e$^-$, 64nV/e$^-$
DC Power consumption	10µW/pix	10µW/pix

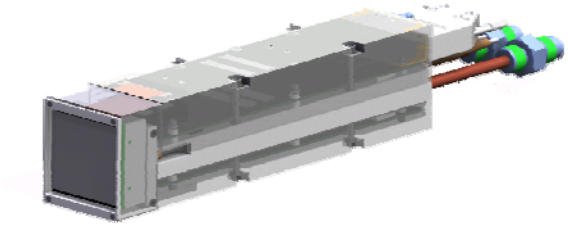

Figure 2. ePix 2x2 camera housing concept.

Considering the limited speed and complexity of ADC architectures that could be implemented in pixels, having an ADC per column, optimizes the performance in terms of conversion and readout time. It also allows the design of fully analog pixels and frees up space in the pixels that can be used for more advanced filtering circuitry. The choice of Sigma Delta converters [4] is a trade-off among sampling rate, resolution, level of digital multiplexing, serialization rate and development time. Sigma Delta converters have the possibility to control the resolution adjusting the oversampling rate, and thus trading resolution for conversion speed. Their intrinsic pseudo-random nature reduces amplitude dependent cross-talk among channels in systems where several ADCs operating at the same time are present. The architecture also implements a dedicated serial control interface that allows handshake as opposed to standard SPI or I2C interfaces. All the required support electronics to perform configuration, calibration and readout of the matrix are also implemented. Columns are divided in 4

banks. To achieve maximum frame rate the output of all ADCs in a bank will be serialized, encoded and transmitted on a single high speed LVDS link. The 4 banks are readout in parallel to speed up the readout process. The acquisition and the readout phase are non-overlapped and are controlled by a single periodic signal (ACQ) whose period defines the integration time. This signal is synchronized to the LCLS beam trigger. During the active part of the ACQ period the charge from the pixels is integrated and sampled. During the inactive period stored data are readout and the system is reset. A power pulsing method is implemented, reducing the power consumption of the various sections of the ASIC during their respective idle states. Support electronics to perform gain calibration per pixel is included together with the possibility to track and correct common mode variations between frames and temperature variations.

3. ePix100 and ePix10k pixel architectures

Figures 3 and 4 respectively show simplified block diagrams of the pixel architecture of ePix100 and ePix10k.

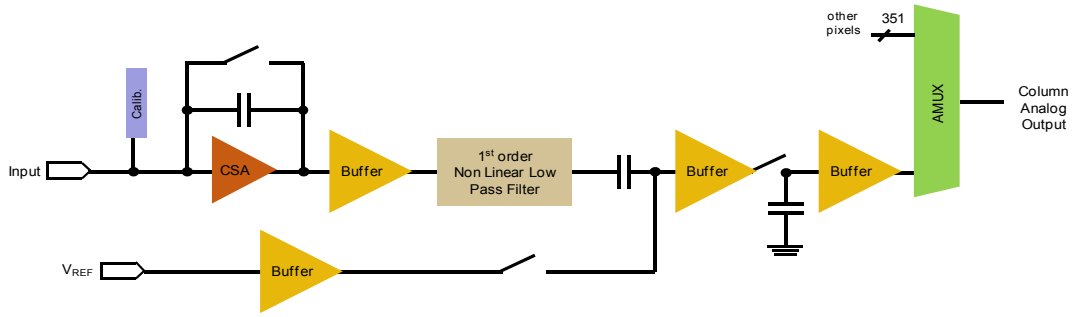

Figure 3. Simplified block diagram of the ePix100 pixel.

Each pixel implements a single stage low noise charge integrator with a pulsed reset, a first order non-linear programmable Low Pass (LP) filter, a correlated double sampler (CDS) and a sample and hold stage followed by a column buffer. Because of the limited area the circuits in the blocks are not complex and small buffers are required to decouple the various sections.

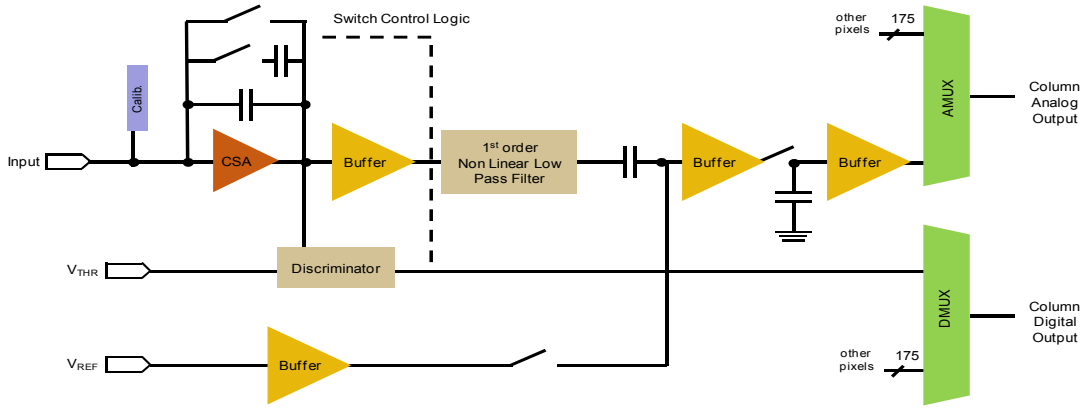

Figure 4. Simplified block diagram of the ePix10k pixel.

In ePix100 noise requirement is dominant and thus noise considerations drive the optimization of the signal chain. In ePix10k the large signal range is the driving requirement. ePix10k implements multiple gain settings and auto-ranging [5]. The auto-ranging system allows reducing dynamically the gain of the pre-amplifier depending on the input signal level and thus extending the dynamic range

without sacrificing the resolution for small signals. The first order LP filter is designed using active resistors to limit the area taken. Active resistors are nonlinear but are optimally sized to produce maximum filtering at low number of photons. The time constant of the filter is continuously programmable by an internal DAC. The CDS stage is used to sample and store the filter output, eliminating the fluctuations due to KTC noise and baseline fluctuations, and to reduce low frequency noise [6]. In this architecture a "quasi-trapezoidal" noise weighting function can be implemented. Figure 5 and 6 show the layout of the two different pixel designs.

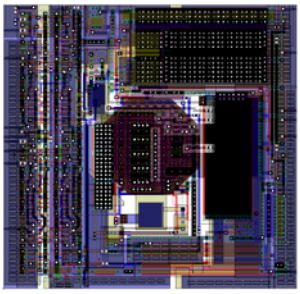

Figure 5. ePix100 pixel 50µmx50µm

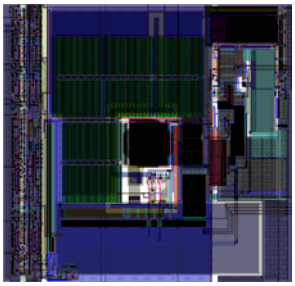

Figure 6. ePix10k pixel 100µmx100µm

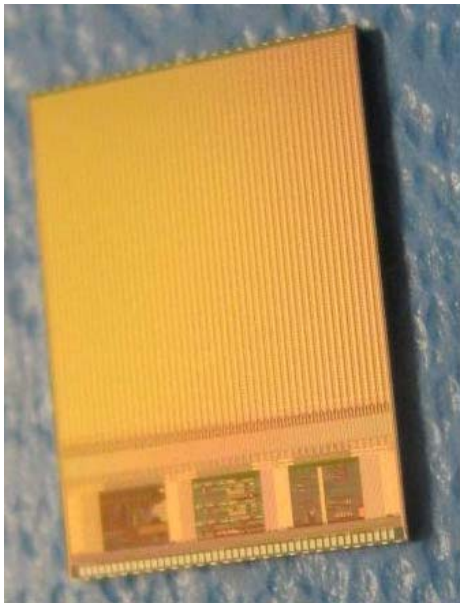

Figure 7. ePix100 96x96 pixel prototype.

The first prototype of ePix100 (figure 7) has been fabricated and tests to assess the performance are underway.

Acknowledgments

SLAC-PUB-15640. Use of the SLAC National Accelerator Laboratory, was supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under Contract No. DE-AC02-76SF00515.

References

[1] Hruszkewycz S O, Sutton M, Fuoss P H, Adams B, Rosenkranz S, Ludwig K F Jr, Roseker W, Fritz D, Cammarata M, Zhu D, Lee S, Lemke H, Gutt C, Robert A, Grübel G, Stephenson G B 2012 *Physical Review Letters* **109** 185502

[2] Boutet S, Lomb L, Williams G J, Barends T R M et al. 2012 *Science.* **337** 362

[3] Hart P, Boutet S, Carini G A, Dragone A, Duda B, Freytag D, Haller G, Herbst R, Herrmann S, Kenney C, Morse J, Nordby M, Pines J, van Bakel N, Weaver M, Williams G, 2012 *NSS-MIC Conference records.* 538

[4] Schreier R, Themes G C 2004 *Understanding Delta-Sigma Data Converters* (New York: Wiley-IEEE Press)

[5] Freytag D, Herbst R, Brau J, Breidenbach M, Frey R, Haller G, Holbrook B, Lander R, Nelson T, Radeka V, Strom D, Tripathi M, 2008 *NSS-MIC Conference records.* 3447

[6] Porro M, Fiorini C, Strüder L 2003 *Nucl. Instrum. Methods, A.* **512** 179