THE HARDWARE IMPLEMENTATION OF THE CERN SPS ULTRAFAST FEEDBACK PROCESSOR DEMONSTRATOR[*]

J. E. Dusatko[#], J. M. Cesaratto, J. D. Fox, J. Olsen, C. H. Rivetta, SLAC, Menlo Park, California, USA
W. Höfle, CERN, Geneva, Switzerland

Abstract

An ultrafast 4GSa/s transverse feedback processor has been developed for proof-of-concept studies of feedback control of e-cloud driven and transverse mode coupled intra-bunch instabilities in the CERN SPS. This system consists of a high-speed ADC on the front end and equally fast DAC on the back end. All control and signal processing is implemented in FPGA logic. This system is capable of taking up to 16 sample slices across a single SPS bunch and processing each slice individually within a reconfigurable signal processor. This demonstrator system is a rapidly developed prototype, consisting of both commercial and custom-design components. It can stabilize the motion of a single particle bunch using closed loop feedback. The system can also run open loop as a high-speed arbitrary waveform generator and contains diagnostic features including a special ADC snapshot capture memory. This paper describes the overall system, the feedback processor and focuses on the hardware architecture, design and implementation.

BACKGROUND

CERN is undertaking an intensity upgrade in their LHC injector chain to allow full exploitation of the LHC at high luminosity [1]. A side-effect of these upgrades is that the planned factor of two increase in SPS beam intensity leads to e-cloud and TMCI driven transverse intra-bunch instabilities.

Much work has been done to understand this phenomenon and develop possible control techniques using simulation and measurements [2,3]. A progression of this R&D effort has been the development of a feedback control demonstrator system [4,5]. This feedback demonstrator system provides a flexible means for which to control and measure the feedback operation. Using this system, we have been able to drive a single bunch into instability and then use feedback to stabilize it.

OVERVIEW OF SYSTEM

The feedback demonstrator system is part of a larger setup that includes an excitation system [6], as shown in Fig. 1. The beam bunch motion is sensed by four exponentially tapered striplines, whose outputs are processed by an analog front end receiver. The receiver sums the individual stripline plates in the horizontal and vertical planes and takes the difference of the summed plane pairs to obtain the bunch displacement signal. This

signal is then further low-pass filtered, amplified and equalized. The last operation is performed to compensate for distortions introduced by the pickup and cable plant. The ADC has an input bandwidth of around 2GHz, which is further limited to 800MHz by the analog front end Bessel low-pass anti-aliasing filter.
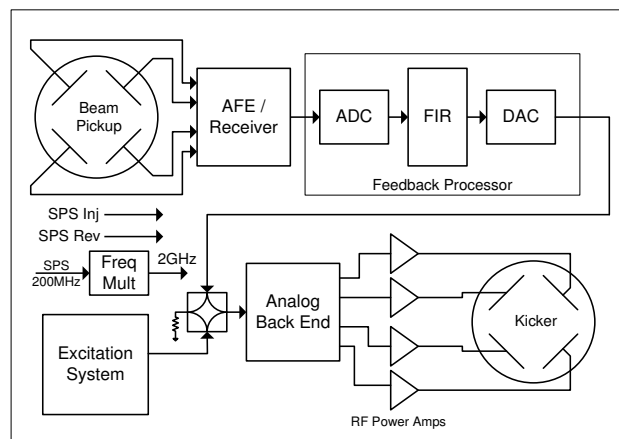

Figure 1: Overall Setup Block Diagram.

The feedback processor converts the analog bunch position signal into the digital domain, performs an algorithmic process on it and then converts it back to the analog domain. The processor's bandwidth is 1.5GHz.

The analog correction signal is then processed by the analog back end block which low-pass filters, amplifies, splits and distributes it to four high power RF amplifiers which drive the kicker structure, applying a corrective field to the beam bunch. The DAC's output bandwidth is limited to 1.5GHz, which is further reduced by the 200MHz bandwidth of the kicker.

The feedback processor output is combined using a hybrid with the output of the excitation system. The latter is essentially a programmable arbitrary waveform generator, which allows us to generate a time-domain drive signal along the same output path. This overall setup allows us to perturb the beam into instability and then correct it with feedback.

Three timing signals are received from the SPS low level RF and timing systems: the 200MHz RF accelerator reference clock (multiplied up to obtain the 2GHz sample clock), the injection marker and the bunch revolution maker. These signals allow us to synchronize sampling, system timing and operation, and enables selection of individual bunches within the SPS batch. Note that the frequency multiplier can select any n*RF harmonic, up to n=10 (2GHz); for our initial studies, we selected n=8 (1.6GHz) to simplify synchronization with the SPS.

FEEDBACK PROCESSOR

The feedback processor is architected as a genera-purpose, single channel reconfigurable signal processor, based around a modular topology that uses both commercial and custom-designed components.

It has been designed to operate in two modes: a) Feedback, where we close the loop around the beam, and b) Excitation, where the system operates exactly as the stand-alone excitation system.

The system processing occurs in a bursted manner, with short periods of high dataflow and computing when a packet of 16 samples is processed (as initiated by the revolution marker), followed by a quiescent period before the correction signal is output as another burst of 16 samples, following the very next revolution marker. Currently, the system only processes a single beam bunch, but will later be expanded to handle multiple bunches.

The physical architecture is based on a motherboard-daughter board topology. The motherboard contains the FPGA and interconnects to the ADC, DAC and support functions via connectors to daughterboards. A block diagram of the Feedback Processor Demonstrator is shown in Fig. 2. This diagram outlines the functional elements of the processor and includes both hardware and FPGA gateware elements. Each major functional section is now described.

FPGA Motherboard

A commercial FPGA motherboard (Dini Group DNMEG_V6HXT) was chosen. It contains a single Xilinx XC6VHX565T, Virtex-6 FPGA. This board is targeted at ASIC verification and high-speed serial I/O applications but was chosen because it contains two high-speed, high-density daughterboard connectors. One connector employs the FPGA Mezzanine Connector (FMC) standard, while the other employs a manufacturer-defined MEG-Array standard. Both connectors provide a large number of impedance controlled differential data and clock signal pairs plus power, facilitating the interconnection of daughterboards. FPGA configuration is via either JTAG or a bit file downloaded from a USB stick inserted into the motherboard.

ADC

The processor uses two Maxim Semi MAX109 2GSa/s, 8-bit ADC devices operating in interleaved mode to give an effective sampling rate of 4GSa/s. The input ADC signal is split using a wideband power splitter. The time interleaving function is achieved by inserting a time delay equal to one sample clock period in one leg of the input signal path (see Fig. 2).

The ADC was originally to be developed as a separate daughterboard. However, due to limited resources a more expedient solution was required. Therefore, the ADC subsystem was implemented using two Maxim Semi MAX109EVKIT evaluation (eval) boards and a custom high-speed cable assembly that mates the eval boards to the motherboard at the FMC connector. The cable assembly was developed in partnership with the Samtec Corporation and contains 78 length-matched 100 Ohm differential micro coax signal pairs. These mate with the motherboard's differential traces, which are loosely
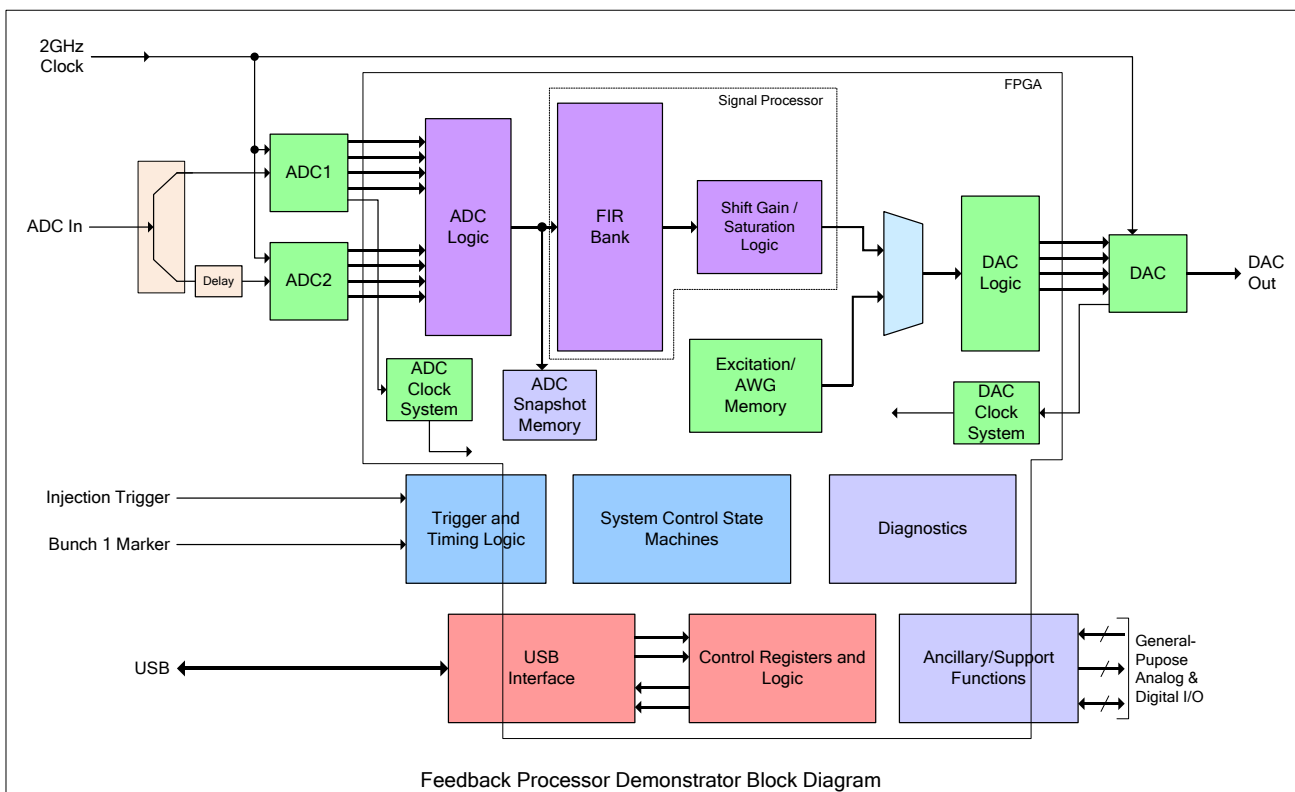

Figure 2: The feedback processor block diagram.

-coupled 50 Ohm transmission lines. The overall cable assembly length is 24 inches. Despite the fact that the eval board's signal connectors are non-impedance controlled 0.1 inch dual row headers, no detrimental mismatch issues were experienced. DC power and the sample clock are routed to each board on separate connectors. Each ADC sends four, 8-bit, 500MSa/s data streams into the FPGA, along with a 250MHz Double Data Rate (DDR) data clock. The four output samples from each ADC device are synchronized with a reset signal from the FPGA, to ensure proper alignment.

DAC

The DAC subsystem is implemented on a custom daughterboard along with the USB interface and ancillary/support functions. This board mates with the MEG-Array connector. The DAC device is a Maxim Semi MAX19693, 4GSa/s 12-bit device used in 8-bit mode (the four LSBs are driven logic zero). The DAC device receives the 2GHz sample clock and uses both edges to generate an effective sample rate of 4GSa/s. It receives four 1GSa/s data streams from the FPGA, while forwarding a 500MHz DDR data clock to it for clocking. The DAC output signal is differential and is converted to single-ended via a wideband transmission line balun. The low-pass reconstruction filter is contained in the Analog Back End subsystem. The sample clock is received and conditioned on board. The DAC device does not provide a reset input to align the four input samples to a consistent sample clock phase. Therefore, alignment is different at each power cycling of the system. This is an accepted condition that will later be resolved by using a phase locked loop to drive the sample clock. A photo of the daughterboard is shown in Fig. 3.
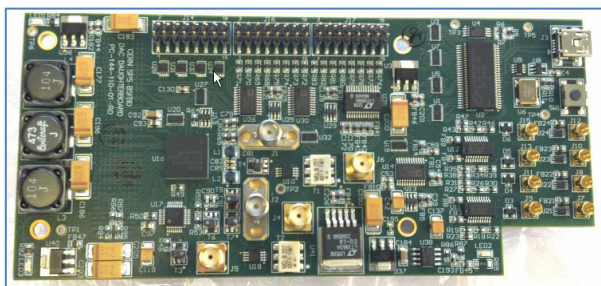

Figure 3: The DAC Daughterboard.

Besides the DAC function, the daughterboard also hosts a USB 2.0 interface, using a Cypress Semi CY7C68013 EZ-USB device. The parallel 16-bit USB data is run to the FPGA along with control signals and the USB-derived 48MHz clock. In addition to the interface, the board also contains four input trigger receivers implemented using bipolar comparators with individually DAC-adjustable thresholds; and four TTL-level strobe outputs capable of driving 50 Ohm loads. These are used for observation of key signals within the feedback processor. Lastly, the board contains eight general-purpose digital and analog (separate ADC in

and DAC out) I/O ports. These are available for use in ancillary and supporting functions.

FPGA Design

The FPGA implements and joins together all of the functional elements of the feedback processor. It handles all of the dataflow and processing from ADC in to DAC out, implements the USB interface to the outside world, and contains all of the control, status, diagnostics and clocking of all data processing, support and housekeeping functions. The major functional blocks are now described.

The ADC parallel data streams are received and clocked into the FPGA fabric via input DDR receiver registers. All 16 ADC data bytes (slice samples) are then de-interleaved and organized into the correct temporal order as one 128-bit data word that is passed into the signal processing block. The ADC data is processed at the data clock frequency in the fabric of the FPGA device.

The signal processor block performs all of the processing functions on the ADC data. It receives the 128-bit word and maps each sample slice into a 16-tap, 16-channel FIR filter bank. There is one channel for each filter slice, with each processed independently. The FIR filters are described by the following relation:

$$y(n) = \sum_{k=0}^{15} h(k)x(n-k)$$

Where each sample, $x(n-k)$ is multiplied by an 8-bit signed coefficient, $h(k)$ and summed, generating the 20-bit signed result, $y(n)$. The filter bank accepts two loadable coefficient sets (one set applies to all 16 filters simultaneously). The coefficient sets are swappable on the fly and can be programmed to run with the desired set for n turns, swap to the other set for m and then back to the original set. This mechanism allows us to dynamically swap between positive and negative feedback coefficients for grow/damp measurements and/or selectively activate/deactivate the feedback. The 20-bit FIR output must be scaled to fit within the 8-bit DAC sample window. This is accomplished with the user-programmable shift gain/saturation block. This block also detects and notifies over- and under-flow conditions. The signal processor runs on the ADC fabric clock.

The DAC logic takes the gain shifted filter data, pipelines and orders it into four 8-bit fast datastreams. The data is up-converted into the fast streams using the FPGA's fast output shift register blocks. The DAC fabric logic is clocked with one half the DAC data clock frequency (250MHz for a 2GSa/s sample clock). Additionally, the DAC can be driven by an internal excitation memory loaded over USB. This enables the feedback processor to run in excitation mode.

The FPGA also implements diagnostic functions including a missing trigger detector and error counter as well as a special ADC snapshot feature. The snapshot selectively records (under user control) a

programmable number of turns of pre-filtered ADC data. This data can then be read out over USB for viewing and analysis. All system dataflow, timing and sequencing operation is coordinated by a set of state machines.

The FPGA contains three clock domains: the ADC, DAC and USB interface. All USB data and control signal clock domain crossings are synchronized to the respective ADC and DAC clocks as needed. The two ADCs provide individual data clocks, but only one is needed inside the FPGA. The ADC and DAC data clocks are processed inside the FPGA using Mixed-Mode Clock Manager (MMCM) blocks that distribute a phase locked version of the ADC and DAC input data clock to the fabric. The MMCM also provides a fine phase adjustment to ensure proper timing margins.

Clock domain crossing synchronization for the processed data is handled by placing the data in a shallow dual clock FIFO and synchronizing the request and acknowledge flags between state machines in each domain.

The FPGA design was developed using pure VHDL coding. Certain functional blocks (FIR filter bank, memories, etc.) were generated using the Xilinx CORE Generator tool. Simulation was done using ModelSim PE and the FPGA itself was synthesized, placed and routed using the Xilinx ISE design suite version 14.

Packaging

The feedback processor demonstrator is packaged in a 7U, 19-inch rack mount chassis. In addition to the boards described above, it also contains the ADC input board, which contains the input power splitter and delay element. It also houses the sample clock RF amplifier and splitter, and the switch-mode power converter. All signal I/O is through the front panel which also contains status and power indicator LEDs. Fans on the motherboard, power converter, ADC boards and chassis itself provide cooling. The unit is powered from the AC mains.

System Software

The chassis is controlled with a GUI based application written in Microsoft Visual Basic (VB). The GUIs interface with it over USB using driver calls. Several offline MATLAB-based tools have been developed to facilitate configuration of the feedback mode, generation of excitation data files, design of the FIR filters, and analysis and display of the ADC snapshot data. Data and configuration settings are exchanged between MATLAB and Visual Basic via text based auto-generated setup files.

SUMMARY AND FUTURE DIRECTION

The feedback processor demonstrator system was used in machine development measurements at the SPS from Nov-2012 to Feb-2013. Several studies were performed, and a wealth of data was collected [7]. This data has helped us verify and fine-tune the simulation models. The results are very encouraging and show feedback control of mode 0, with observation of higher order modes as well. Figure 4 shows the feedback in action on an SPS bunch (16 samples over 40 turns).
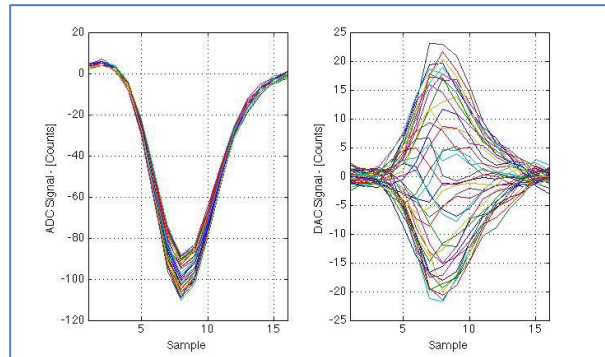

Figure 4: Feedback system beam bunch signal input (left) and correction output (right).

Moving forward during the CERN long shutdown, we plan on upgrading and enhancing this demonstrator system. This work includes: the processing and control of multiple bunches, orbit offset correction, advanced filter structures and expanded operating modes.

Being reconfigurable, it offers flexibility for use in other accelerator applications. As a prototype, it has allowed us to develop and verify techniques which will lead to a final solution for the SPS, with possible application to other accelerators as well.

REFERENCES

[1] E. Shaposhnikova, "Intensity Upgrade Plans for CERN-LHC Injectors," 42nd Advanced ICFA Beam Dynamics Workshop Nashville, TN, 2008, CERN-AB-2008-065.

[2] C. Rivetta et al., "Mathematical Models of Feedback for Control of Intra-Bunch Instabilities Driven by E-Clouds and TMCI", PAC2011, New York NY, WEP079.

[3] K. Li et al., "Modelling and Studies for a Wideband Feedback System for Mitigation of Transverse Single Bunch Instabilities", IPAC2013, Shanghai, China, WEPME042.

[4] J. D. Fox et al., "A 4 GS/s Feedback Processing System for Control of Intra-Bunch Instabilities", IBIC2013, Oxford UK, TUBL2.

[5] J. Dusatko et al., "A 4GSa/s Instability Feedback Processing System for Intra-Bunch Instabilities", IPAC2013, Shanghai China, WEPME059.

[6] J. D. Fox et al., "A 4.2GS/s Synchronized Vertical Excitation System For SPS Studies – Steps Toward Wideband Feedback", IPAC2012, New Orleans, May 2012, WEPPR090.

[7] J. D. Fox et al., "First results and analysis of the performance of a 4 GS/Sec intra-bunch feedback system at the SPS" IPAC2013, Shanghai China,WEPME060.