

FABRICATION AND MEASUREMENTS OF A SILICON WOODPILE ACCELERATOR STRUCTURE

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Abstract

We present results for the fabrication of a silicon woodpile accelerator structure. The structure was designed to have an accelerating mode at $3.95 \mu\text{m}$, with a high characteristic impedance and an accelerating gradient of 530 MeV/m . The fabrication process uses standard nanofabrication techniques in a layer-by-layer process to produce a three-dimensional photonic crystal with 400 nm features. Reflection spectroscopy measurements reveal a peak spanning from three to five microns, and are show good agreement with simulations.

INTRODUCTION

Advancements in laser technology and commercialization of this technology has driven interest in applying lasers to particle acceleration. One approach is to use dielectric structures with low power, high rep rates lasers. This approach requires no plasma, uses small commercially available laser systems, and structures that can be manufactured using current nanofabrication techniques. Dielectric materials are used to confine the electric fields of the optical beam in much the same way that traditional RF accelerators confine microwave frequencies in accelerating cavities. Dielectric materials are advantageous in that they allow one to reach higher electric fields before breakdown occurs, but also pose challenges in confining the radiation due to the lack of hard boundary conditions that are inherent with metallic structures. Various schemes such as planar and cylindrical Bragg structures [2], photonic bandgap (PBG) fibers [3], and three-dimensional photonic crystals (3D PhC) have been explored as candidates accelerator structures. We focus here on the design, fabrication, and characterization of a specific type of 3D PhC, called a woodpile structure.

A woodpile structure consists of rods of a high index material stacked up in a fashion depicted in Figure 1. This arrangement has been shown to have a large 3D bandgap [1]. That is, light of a certain range in frequencies is completely reflected from this structure due to constructive interference of the reflected radiation and destructive interference of the transmitted waves. This is true for light incident on this structure in any direction. By removing material from a region of the lattice a defect is formed. Radiation can now be confined to this defect and manipulated by adjusting the geometry of the surrounding lattice. The mode depicted in Figure 1 shows a defect that has been optimized for an

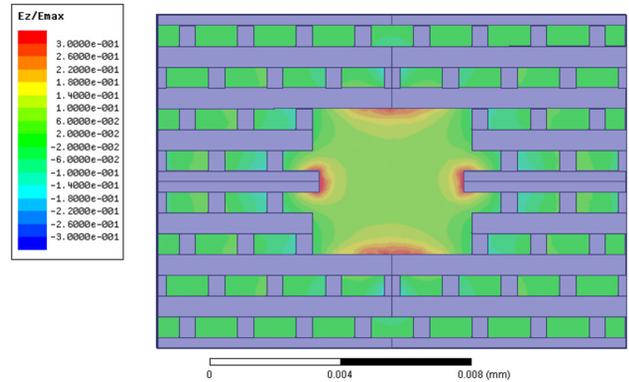


Figure 1: Field plot of E_z normalized to the maximum electric field for the speed-of-light accelerating mode in the woodpile accelerator structure. The parameters for this mode are listed in Table 1.

accelerating mode with speed-of-light phase velocity and a significant longitudinal electric field component. Much of the original design and optimization was carried out by Cowan [4], and is built upon here.

Table 1: Parameters for a 17 Layer Silicon Woodpile Accelerator Structure

Structure Properties	Value	Units
Lattice Period (a)	1.45	μm
Rod Width (w)	406	nm
Layer Height (h)	513	nm
Defect Size	3.6×3.6	μm
n_{Si}^*	3.46	
Damage Fluence* (F_{th})	0.314 [5]	$\frac{\text{J}}{\text{cm}^2}$
*at $\lambda = 3.9 \mu\text{m}$		
Mode Properties	Value	Units
E_z/E_{max}	0.14	
Q	804	
v_g	0.263	c
Z_c	326	Ω
Z_d	44.3	Ω
E_{acc}	530	MeV/m

Table 1 shows a list of parameters for this particular mode. The actual size of the structure, referenced to the lattice period, a, can scale freely with wavelength, but is ultimately restricted by fabrication limitation, or achiev-

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able or desirable laser wavelength. Here we focus on a silicon based structure with a lattice period of $1.45 \mu\text{m}$, and a mode frequency of 75.9 THz , or $3.95 \mu\text{m}$ free-space wavelength. Properties of the accelerating mode depicted in Figure 1 are computed from eigenmode simulations performed in HFSS. An accelerating gradient of 530 MeV/m is computed based on the field profile and damage fluence of silicon at $3.95 \mu\text{m}$. The damage impedance and characteristic impedance are defined as

$$Z_d = \frac{E_{acc}^2}{2u_{max}c}, \quad Z_c = \frac{E_{acc}^2\lambda^2}{P},$$

where E_{acc} is the on axis longitudinal electric field, u_{max} is the maximum energy density in the material, and P is the total power in the mode. The high characteristic impedance of this mode is a result of strong confinement of the fields and good coupling between the fields and the electron beam. The full 3D bandgap also provides a way to design couplers directly integrated in the structure and fabricated simultaneously with the rest of the structure.

FABRICATION

The fabrication method used is derived from a technique pioneered by Lin and Flemming [6], and is depicted in Figure 2. Other fabrication methods, such as Direct Laser Writing [7] or fusion bonding of GaAs substrates patterned by electron beam lithography [9] are worth mentioning as possible alternatives that could offer a means towards smaller scale feature sizes. The layer-by-layer method used in this process is based on mature techniques that could be easily implemented in a mass production fabrication facility using relatively mature processing techniques.

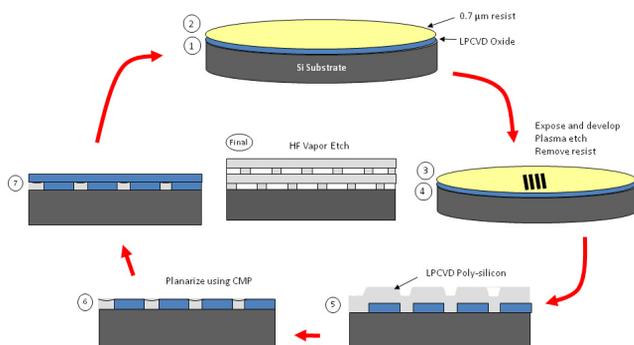


Figure 2: Fabrication process for the layer-by-layer approach developed for woodpile structure. Details are presented in the text.

The structure is built up one layer at a time. Alignment between successive layers is critical to ensuring a high quality bandgap, and is achieved using an ASML PAS5500 i-line stepper with a 3σ alignment accuracy of 60 nm , or 0.04λ . A layer of silicon dioxide is first deposited on the wafer using a low pressure chemical vapor

deposition (LPCVD) (step 1). Uniformity across the wafer is typically within 2% and accuracy of the layer thickness is typically within 5% . The oxide is used as a matrix into which the silicon is deposited, but the oxide thickness ultimately determines the thickness of the silicon layer so is a critical parameter to control.

The features for the given layer are then patterned into the oxide using standard optical lithography. A thin $0.7 \mu\text{m}$ thick layer of layer of Shipleys 955 resist is spun onto the surface of the oxide layer (step 2). The ASML stepper is then used to expose the desired layer image into the resist (step 3). Each layer is designed and patterned on a mask that is imaged with a 5:1 demagnification onto the wafer, with a minimum feature resolution specified at 450 nm . The minimum features for this structure were slightly below this spec, targeted for 406 nm , or 0.28λ .

Once the wafers are exposed and developed the image patterned into the resist is transferred into the oxide through magnetically enhanced reactive ion etching (MERIE) using Applied Material P5000 etcher (step 4). This process balances a chemical etch using CHF_3 and CF_4 with a physical one using Ar, in order to achieve an etch profile with near vertical side walls and sufficient selectivity.

The resist is then removed and a layer of poly-silicon is deposited using LPCVD of SiH_4 at 620°C (step 5). The layer thickness for the poly-silicon is roughly targeted for 150% of the oxide layer to ensure complete filling of the patterned features and a planar top surface of poly-silicon.

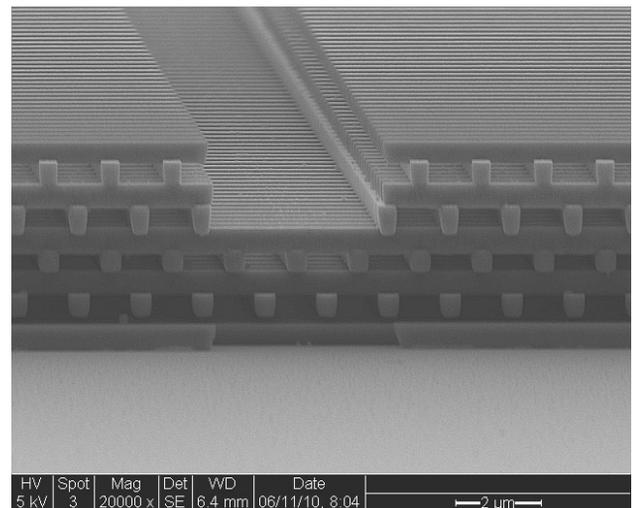


Figure 3: A successfully fabricated 9 layer silicon woodpile accelerator structure with a defect. This structure will be bonded to an eight layer structure to form an complete 17 layer structure with a confined defect channel.

The poly-silicon is then chemically mechanically polished (CMP) down to the surface of the oxide (step 6). A 3:1 poly-si:oxide polish rate selectivity is achieved using KOH based S10 slurry from Eminess, and the oxide surface is detected using an end-point detection based on a friction monitor in the polishing head. The uniformity af-

ter polishing is typically better than 5%. The wafers are then decontaminate for KOH, and the process is started all over again (step 7).

Once the desired number of layers are achieved the wafers are annealed to reduce the intrinsic stress in the poly-silicon. Poly-silicon is slightly tensile stressed as deposited, and must be annealed to prevent delamination between the layers. This anneal does not relieve the high compressive stress in the oxide due to different thermal expansion coefficient of oxide and silicon. This stress is balanced as the oxide is deposited uniformly on the front and backside of the wafer during the deposition. Vapor HF is used for the final release, resulting in a free standing structure of silicon, as depicted in Figure 3.

OPTICAL CHARACTERIZATION

The fabrication quality was assessed through optical spectroscopy measurements. A fourier transform infrared spectrometer (FTIR) from Thermo Fisher was used to measure the transmission and reflection for structures at successive points in the fabrication process. Figure 4 shows reflection spectra for four, six, eight, and nine layer structures demonstrating a clear bandgap spanning from three to five microns. The spectra are normalized to the reflectivity of a gold mirror included for reference.

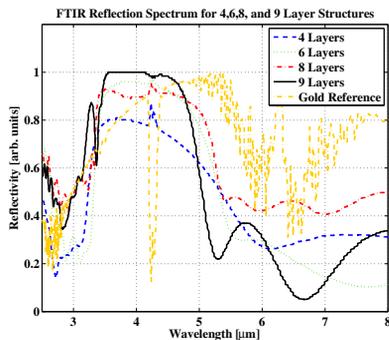


Figure 4: Reflection spectroscopy of four, six, eight, and nine layer structures reveal a clear bandgap between three and five microns.

A simple code based on plane wave expansion in a two-dimensional plane and scattering matrix method [11] for transmission from one layer to the next was developed to analyze the measured spectroscopy data. Using SEM images of the fabricated structures to measure rod width, layer thickness, alignment and rod taper, an accurate model of the structure was developed and good agreement with spectroscopy measurements is shown in Figure 5. Center bandgap wavelength agrees to within 3% between the simulation and the measurement.

CONCLUSION

We have developed a method for fabricating a silicon woodpile structure designed with an accelerating mode at

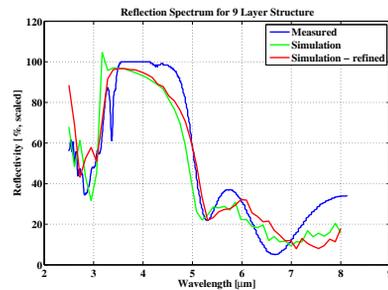


Figure 5: Reflection spectra for the 9 layer structure compared with scatter matrix based simulations of a structure with ideal design parameters, and a model that was refined using SEM images of the actually fabricated structures.

3.95 μm . The structure was characterized using reflection spectroscopy and good agreement between simulations and measurements are found. An optical parametric oscillator (OPO) with a tunable output from 3 to 5 μm is currently being constructed using a periodically poled lithium niobate crystal pumped with a Nd:YAG laser. The OPO will be used to probe the defect modes of the resulting structure and quantify coupling efficiency, transmission losses, and directly measure the damage threshold for this structure. Electron beam experiments will also be done using the NLCTA 60 MeV beamline at SLAC.

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