SLAC-PUB-16682

FABRICATION AND MEASUREMENT OF DUAL LAYER SILICA GRATING STRUCTURES FOR DIRECT LASER ACCELERATION*

E.A. Peralta†, R.L. Byer, Stanford University, Stanford CA 94305, USA
E. Colby, R.J. England, C. McGuinness, K. Soong, SLAC, Menlo Park, CA 94025, USA

Abstract

We present our progress in the fabrication and measurement of a transmission-based dielectric double-grating acceleration structure. The structure lends itself to simpler coupling to the accelerating mode in the waveguide with negligible group velocity dispersion effects, allowing for operation with ultra-short (fs) laser pulses. This document describes work being done at the Stanford Nanofabrication Facility to create a monolithic guided-wave structure with 800 nm period gratings separated by a fixed subwavelength gap using standard optical lithographic techniques on a fused silica substrate. An SEM and other characterization tools were used to measure the fabrication deviations of the grating geometry and simulations were carried out in MATLAB and HFSS to study the effects of such deviations on the resulting accelerating gradient.

INTRODUCTION

The transmission-based dual layer grating structure [1] is an excellent candidate structure for laser-driven dielectric accelerator since it allows the structure to be optically pumped perpendicular to the electron beam channel, avoiding the inherent group velocity mismatch problem present in co-propagating schemes. Aside from a simpler coupling of the laser power into the structure, this geometry minimizes dispersive effects since the fields traverse very little material, allowing the structure to be driven by ultrashort high-power laser beams. Also, as a traveling wave structure with no energy storage (no optical "Q"), the exposure time to high fields is reduced, enabling significantly higher gradient operation.

The grating structure acts as a longitudinally periodic phase mask that produces a SOL TM space harmonic on axis. As seen in Figure 1, the resulting fields will accelerate a passing electron bunch when the phase of the input field is properly chosen. Previous simulations [1] show that a grating structure with a vacuum channel gap smaller than the driving optical wavelength can achieve significant acceleration gradients of up to 1/4 of the maximum field sustained by the structure. Recent measurements [2] show that the damage threshold of these gratings is 1.6 J/cm^2 which means that a 1ps pulse could produce a 1.1 GeV/m unloaded acceleration gradient with a 50% safety margin.

* Work supported by department of energy contracts DE-AC02-76SF00515 (SLAC) and DE-FG06-97ER41276

† eperalta@stanford.edu

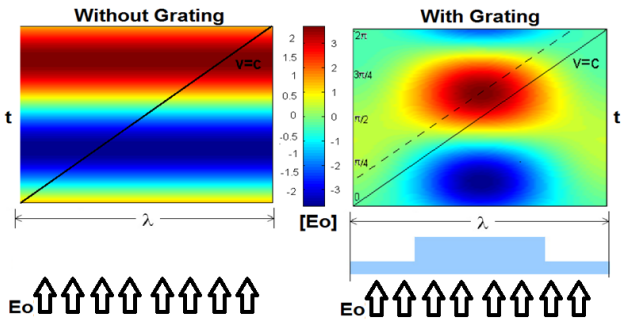

Figure 1: Grating structure principle of Operation: each grating pillar provides a π phase delay such that at the right phase the e-beam experiences net acceleration.

FABRICATION

The process to fabricate the dual layer grating structures has been purposely designed to employ standard CMOS techniques available at the Stanford Nanofabrication Facility (SNF). By avoiding e-beam lithography and focused ion beam etching and choosing instead to develop optical lithography and reactive ion etching techniques we have reduced the complexity and expense of the process, allowing for high throughput and reproducibility. The current process, illustrated in Figure 2, aims to fabricate a proof-of-principle structure designed to operate at the 800nm wavelength (λ) of a high power Ti:Saph laser. It starts by Magnetically-Enhanced Reactive-Ion-Etching (MERIE) of a binary, λ-period grating on the silica substrate (step 1) followed by deposition of a spacer layer (step 2 or 2*) that determines the separation between the two gratings. The etch depth and spacer thickness had been previously determined using 2D FDTD simulations to maximize the resulting acceleration gradient; these were found to be .9λ (720nm) and $\sim \lambda/4$ (200nm), respectively [1].

Recent simulations show that the even when the two gratings are at their worst longitudinal alignment (with the gratings off by $\lambda/4$), the resulting accelerating gradient can still reach up to 75 % of the maximum achievable value [3]. However, a study of the effect of such misalignment on the beam quality has not yet been finalized. Nevertheless, two fabrication strategies are being pursued. The shorter process requires only one additional step, but has larger overlay misalignment. It consists of e-beam evaporation deposition of a 2nm layer of chrome as an adhesion layer followed by a 100nm layer of gold (step 2*) with the gratings initially covered by photoresist and cleared out via lift-off.

This material is based upon work supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under Contract No. DE-AC02-76SF00515.

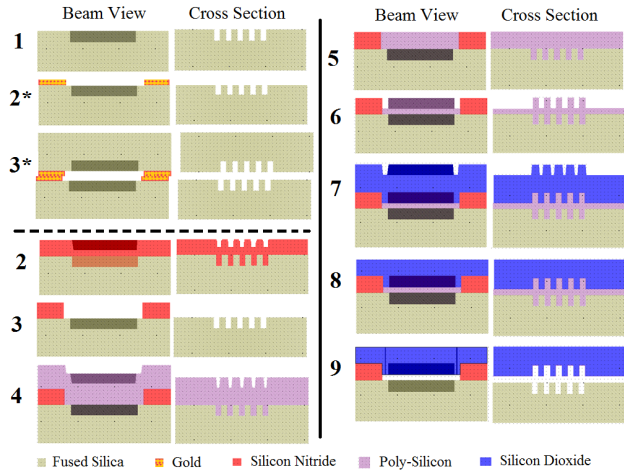

Figure 2: Fabrication Process for the dual layer grating structure. Steps described in the text.

Two such wafers are subsequently aligned and bonded by thermocompression to form a finished structure (step 3*), however the alignment of the top and bottom gratings can be off by up to 10s of microns as determined by the tolerance of the bonding tool.

A more precise structure can be fabricated by relying on the layer-to-layer overlay accuracy during the lithography steps since the i-line exposure system stepper has a manufacturer specification of 60 nm alignment accuracy (3σ). In this case the spacer film is a 1120nm-thick, Low-Pressure-Chemical-Vapor-Deposited (LPCVD) nitride film (step 2) which is subsequently removed from the grating area by wet etching in a phosphoric acid bath at 155^{o}C (step 3). Next, a 1840nm thick layer of poly-silicon is LPCVD-deposited (step 4) and subsequently polished down to the height of the nitride layer (step 5) via chemical-mechanical-polishing (CMP). The poly-Si is then MERIE-etched to form a template for the second grating (step 6) which is filled in by an LPCVD-deposited silicon dioxide layer (step 7), followed by CMP (step 8). Lastly, the vacuum channel is created by a XeF_2 vapor etch (step 9) which etches poly-Si very selectively over oxide.

RESULTS

The i-line stepper's manufacturer-specified 400 nm minimum feature size can typically be obtained with the use of SPR 955-CM i-line resist spin-coated on Si wafers. However, it took significant effort to achieve this feature size on the fused-silica substrates since the material is transparent at the exposure wavelength (365nm), leading to multiple reflections in the substrate which result in a significant increase of the exposure intensity in the resist.

Three different resist were explored before arriving at the correct process: SPR 955 coated at .7 μm (the standard for small feature work on Si), SPR 3617m (dyed for use with clear substrates) coated at 1 μm, and a 2:1 diluted version of SPR 3617m to allow thinner spun films. To determine the right exposure energy a resolution test pattern (shown in Figure 3a is patterned on the resist with a linearly varying exposure energy across the wafer.

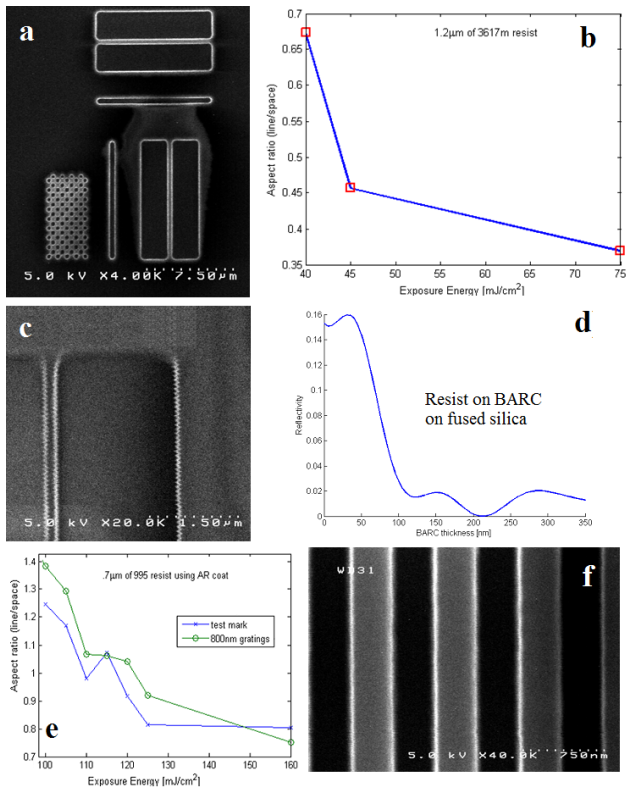

Figure 3: Lithography optimization: a) Test pattern, b) exposure trend with standard resists, c) sample over-exposed pattern, d) Reflectivity improvement using AR coat, e) exposure trend with AR coat applied, f) sample exposed grating pattern using AR coat.

A pattern was considered properly exposed when the lines and spaces measured the same width (aspect ratio of 1). The overall observed trend can be summarized by Figure 3b which shows the variation of aspect ratio as a function of exposure energy. To obtain a proper exposure energies below 40 mJ/cm^2 were required but these were not possible on our stepper. Figure 3c shows a typical over-exposed pattern with the line measuring half its design width and also showing jagged edges.

In order to properly expose the resist on the clear substrate we resorted to using an anti-reflective coating, BARLi II 200, which is highly absorptive at the exposure wavelength and thus can virtually eliminate all back-reflections when the right thickness is used ($\sim$ 200nm), as shown in Figure 3d. The resulting exposure trend is shown in Figure 3e where one can see that aspect ratio 1 structures can now be patterned. One such structure, exposed with 115 mJ/cm^2 is shown in Figure 3f.

With a resist mask properly patterned we were able to perform MEREI etching of the first grating layer. The optimal recipe for a highly anisotropic etch with optimal side

wall profiles in SiO_2 had previously been determined to have a flow, pressure, magnetic field and RF settings of 25 sccm CHF_3, 50 sccm CF_4, 100 sccm Ar, 30 mTorr, 60 Gauss, and 500 W. An etch recipe to remove the 200nm AR film prior to the main etch was also formulated: 10 sec etch with an O_2 flow of 100 sccm at 150 mTor, 60 Gauss, and 500 W. Lastly, to characterize structure etching we patterned 1mm x 1mm gratings, etched, and diced them to measure the grating width and depth from SEM images of cross-sections like the ones shown in Figure 4. Typical values from the first round of structures etched for 210 sec were $w = 349 \pm 16$nm and $d = 550 \pm 31$nm.

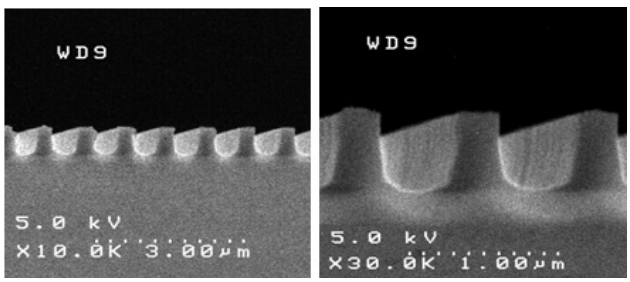

Figure 4: Cross-section of an etched 800nm grating.

We can see from Figure 4 that the grating geometry is not perfectly rectangular. Nevertheless, recent FDTD simulations show that significant acceleration gradients up to 60% of the maximum achievable value can be obtained from this very geometry, despite the rounded edges [3], and up to 73% can be achieved once the optimal groove depth is reached. With this in mind, device-type grating fabrication was started.

The proof-of-principle structure was designed to be 1mm long given the maximum distance for which the 60 MeV beam at the NLCTA remains focused to a few μm spotsize, and 100μm wide to facilitate alignment of the electron and laser beams with the structure while avoiding collapse of the suspended grating. The structure also includes alignment marks visible with a 5X microscope and vernier marks to determine grating misalignment. The structure was etched in the manner mentioned above, but for 275 sec instead of 210 sec to achieve the right depth of 720 nm, and is shown in Figure 5a at 5X magnification and in 5b at 6000X.

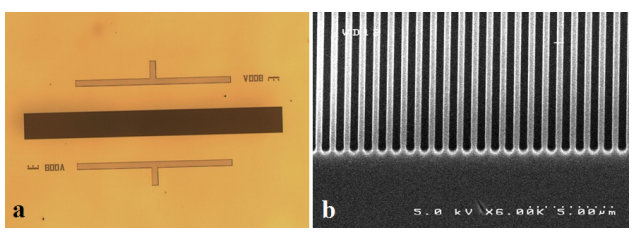

Figure 5: Bottom layer of the accelerator structure.

Next, the silicon nitride layer was LPCVD deposited at 850^{o}C with gas flows of 30 sccm NH_3 and 157 sccm $SiCl_2H_2$ for 135 min, and was measured to be 1142 $\pm$ 20nm thick. However, the film was highly stressed and developed cracks throughout the wafer. Despite this shortcoming, we continued the fabrication process while we develop a recipe to produce low-stress nitride films on silica. This will be done at lower temperatures since most of the stress is a result of thermal expansion since the two materials have significantly different thermal expansion coefficients.

Since a selective etch of silicon nitride in phosphoric acid requires an oxide mask we performed an LPCVD oxide deposition using a standard low temperature oxidation (LTO) recipe at 400^{o}C for 4min. We aimed for 56nm of oxide based on a phosphoric acid etch selectivity of 20:1 (nitride:oxide) and obtained a film 49.6 $\pm$ 8.4 nm thick. The oxide mask was etched for 11 sec by the same MERIE recipe previously described. Based on a SNF user's measured etch rate of 3.4 nm/min, the wafer was then etched in phosphoric acid for 326 min, allowing for a slight over etch to ensure all the nitride is removed from the grating regions. A 5X and 50X image of the resulting structure is shown in Figure 6c and 6d, respectively, where it is evident that the vacuum channel has been formed.

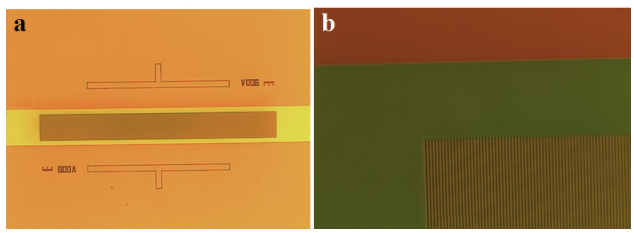

Figure 6: Bottom layer of the accelerator structure with nitride spacer layer and vacuum channel in place.

CONCLUSION

We present initial results on the first steps of a process to fabricate an accelerator structure with the use of only CMOS-compatible techniques. A complete structure will be finished within the next few months following process steps 1-3* mentioned in the text. Fabricated as such, this structure could produce an unloaded acceleration gradient of 600MeV/m at a 50% safety margin.

REFERENCES

[1] T. Plettner, P.P. Lu, and R.L. Byer, "Proposed few-optical cycle laser-driven particle accelerator structure," Phys. Rev. Lett. STAB, 9, 111301 (2006)

[2] K. Soong, et al, "Experimental Determination of Damage Threshold Characteristics of IR Compatible Optical Materials", PAC 11, MOP095 (2011)

[3] K. Soong, E. A. Peralta et al, "Simulation Studies of the Dielectric Grating as an Accelerating and Focusing Structure", PAC 11, MOP104 (2011)