

# BOOSTER RF UPGRADE FOR SPEAR3\*

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## Abstract

SLAC's Stanford Positron Electron Asymmetric Ring (SPEAR3) Booster Radio Frequency (RF) system was recently upgraded where the existing klystron providing RF power to a 5-cell cavity was replaced with a Solid State Amplifier (SSA) [1]. The Low Level Radio Frequency (LLRF) Controls to drive the SSA was provided by a high performance Field-Programmable Gate Array (FPGA) based system built on SLAC's Advanced Telecommunications Computing Architecture (ATCA) modules. RF Cavity Tuner Controls were replaced with EtherCAT-based stepper motor controller. New hardware was designed and built for programmable logic controller (PLC) based Machine Protection System (MPS). Fast digitizers to sample and acquire LLRF signals were implemented in a LinuxRT Server. All of these required new controls software implementation. This paper describes the controls associated with each of the above hardware upgrades.

## BOOSTER RF UPGRADE CONTROLS SYSTEM

The controls layout of the upgraded Booster RF system is shown in Figure 3. The main components are the Experimental Physics and Industrial Control System (EPICS) Input/Output Controller (IOC) controls for the SSA, ATCA, PLC MPS, Booster RF Cavity Tuner and the PCIe Digitizer. Each of these is described below.

### EPICS IOCS

The software controls for all the new hardware described above are via EPICS Soft IOCs running either on a Linux or LinuxRT (Real Time Linux) Server. All IOCs provide the following generic functions:

- Alarm setup capabilities and alarm handling notifications.
- EPICS Process Variable (PV) archival for History plots.
- Save/restore values on IOC boot up.
- Monitoring of processor load, memory usage and IOC heartbeats.
- Extensible Display Manager (EDM) display panels for operator control.
- Message logging.

In addition, each IOC provides functions specific to the hardware to which it interfaces.

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## SSA CONTROLS

The EPICS Soft IOC for SSA controls provides the following functions:

- Control of the SSA over the EPICS Channel Access (CA) network. This includes SSA ON/OFF, set operating mode to either Continuous Wave (CW) or Pulse mode, RF Operate or Standby mode, set DC Power Supply output voltage levels, enable/disable individual power supplies.
- 10 Hz Digital and Analog status updates of the SSA.
- SSA Internal and External Fault detection and Fault Reset capabilities.
- Read SSA Error Codes and provide appropriate alarms.

### SSA IOC

The IOC interfaces with the SSA via the MODBUS protocol based network device. MODBUS is an application layer Messaging protocol in OSI model based on Client-Server communication. The Server in SSA's Main Controller Unit (MCU) supports MODBUS communications via on-board embedded Ethernet network device. The EPICS Soft IOC is the Modbus Client and runs on a Linux Server. The MODBUS communication protocol is over TCP/IP and uses the standard port 502. During development, "modpoll" application which is a MODBUS test utility was used for in-house SSA testing and Factory Acceptance tests. EPICS support MODBUS within the "Asyn" framework [2]. The application for the Soft IOC uses this Asyn based EPICS Module "modbus".

MODBUS supports several Data Types. The SSA uses only the 'Single bit' and '16-bit Register' Data Types. The communication between the Client (IOC) and the Server (SSA) consists of Request Messages sent from the IOC to the SSA and Response Messages received from the SSA by the IOC. The Request Message reads from or writes to 16-bit Modbus addresses defined by the SSA. The data transfer type is described as an 8-bit MODBUS function. EPICS MODBUS supports eight function codes of which the SSA uses only two function codes:

- Function Code 3: Read 16-bit SSA Registers
- Function Code 6: Write 16-bit SSA Registers

SSA Modbus I/O addresses are contiguous 16-bit Registers and begin from address 1. Spear3 Booster RF IOC currently has access to slightly over 400 SSA addresses. Each EPICS MODBUS Read operation is limited to transferring 125 16-bit words at a time. Write operations are limited to transferring 123 16-bit words. SSA responds to every Read or Write Request Messages from the IOC with a Response Message containing valid

data if successful or error codes. The IOC receives analog information from the SSA such as temperature, voltage, and fan speed etc. via Analog Input (AI) Database (DB) records. These records have their SCAN fields set to “I/O Intr” and are processed when Response Messages from the SSA are received in response to periodic polling via Request Messages. SSA Digital status PVs are constructed from the 16-bit AI values. Analog Output (AO) records are used to write set points to the SSA such as threshold limits and desired voltage. Binary Output (BO) records are used for single-bit operations such as SSA ON/OFF and correspond to a single bit defined within a 16-bit word.

The EPICS EDM panel which is the User Interface of the SSA for the operators is shown in Figure 1.

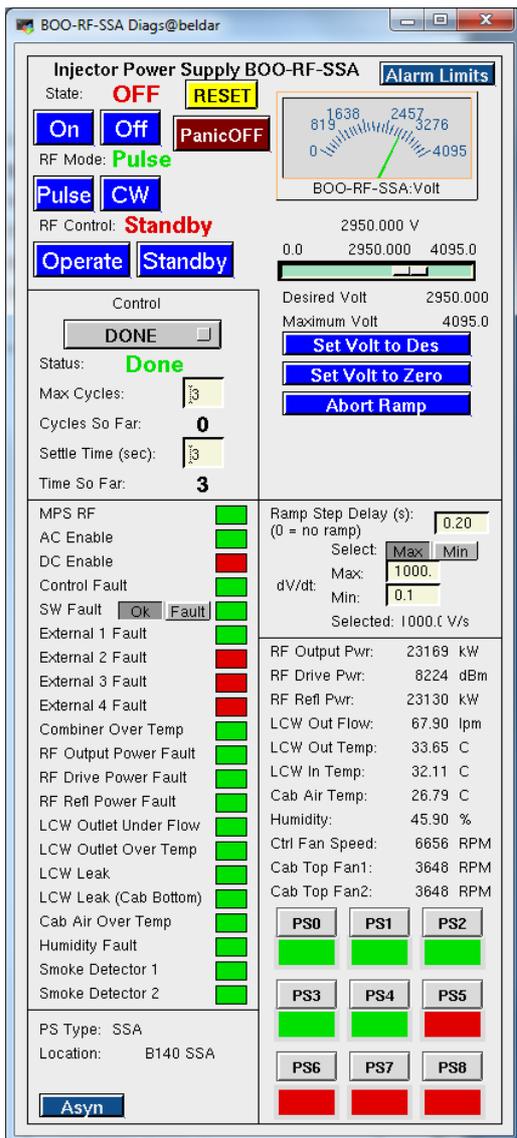


Figure 1: SSA Controls interface.

## ATCA LLRF CONTROLS

The LLRF controls comprises of a High Performance ATCA system consisting of an ATCA chassis and a SLAC-built custom ATCA carrier board with Advanced Mezzanine Card (AMC) LLRF daughter boards custom-built for the SPEAR3 Booster RF frequency. The ATCA system provides the LLRF drive to the SSA via the Digital to Analog Conversion (DAC) AMC1 module and provides RF Phase and Amplitude Fast Feedback (FF) controls using the RF signals read by the fast digitizer in the Analog to Digital(ADC) AMC0 module.

### ATCA LLRF IOC

The LLRF algorithms run on the FPGA while an IOC running on the LinuxRT Server is used for communicating with the ATCA system. The main purpose of this IOC is to provide a User Interface to configure the FPGA and the AMC Modules and to perform periodic acquisition of RF waveforms for diagnostics purposes such as shown in Figure 2.

### CPSW

The communication between the FPGA and the IOC is via a custom protocol “Common Platform Software” (CPSW) [3][4] over Ethernet/UDP across the fibre. The IOC uses an Asyn Port Driver based EPICS module that is layered over CPSW. This module provides support for the YAML definitions of the registers inside the FPGA which is used to auto-generate the EPICS PVs. A different Soft IOC running on the Linux Server provides Intelligent Platform Management Interface (IPMI) based monitoring and controls of both the LinuxRT Server and the ATCA chassis.

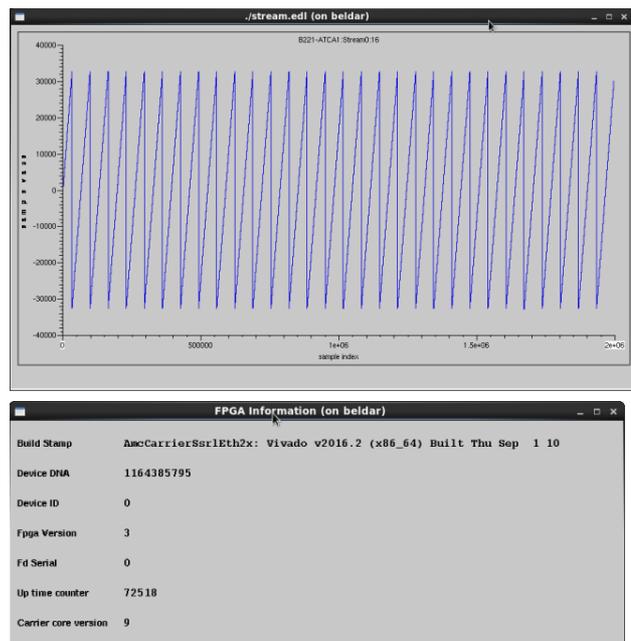


Figure 2: ATCA LLRF Controls interface



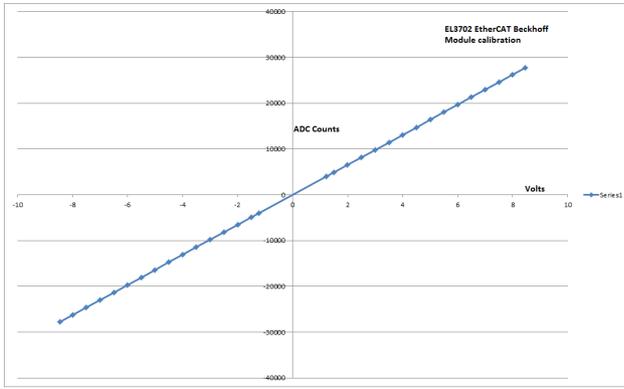


Figure 4: Booster RF Cavity Tuner Motor Calibration.

The IOC uses EPICS Asyn Port Driver layered over the EtherCAT fieldbus scanner software. Two Asyn Driver ports are created corresponding to cell1 and cell5 tuner motor driver, and one for the bus master status. EPICS motor PVs are automatically generated from the device names assigned in the EtherCAT chain description XML file.

The Cavity Tuner Controls User Interface is shown below in Figure 5.

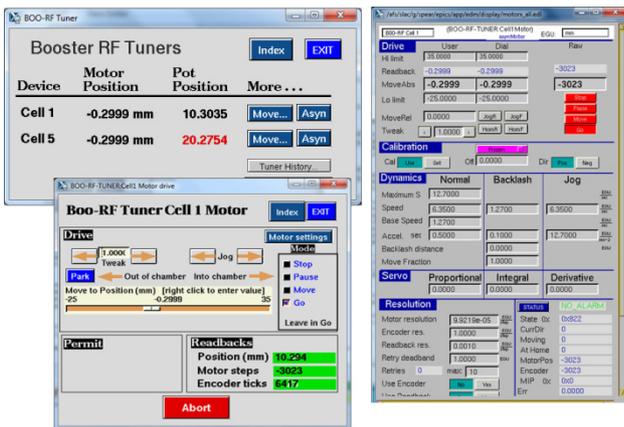


Figure 5: Cavity Tuner Controls interface.

## PCIe DIGITIZER GTR CONTROLS

There are several Booster RF signals whose phase and amplitude need to be monitored continuously to keep track of the health of the overall system even if they are not used in LLRF feedback. The “Gain Phase Detector Chassis” was built to measure the amplitude and phase of such signals and have them monitored via a medium-speed digitizer card in the LinuxRT Server. When triggered, the General Standards 16ai64ssa PCIe ADC digitizes the envelopes of the amplitude and phase of the LLRF signals such as the forward and reverse powers from the SSA and the 5-cell Booster RF cavity probes. This 16-bit 64-channel ADC board is installed in the Server.

## PCIe GTR IOC

The digitizer IOC uses an EPICS Asyn based Generic Transient Recorder (GTR) [8] module to interface with and configure the digitizer driver and to acquire the input signal waveforms. The following GTR configurations are supported:

- Mode: “Post Trigger” or “Disarm”. In Post Trigger mode, the digitizer will start sampling the input signals when a trigger is received. It will not sample when it is “Disarmed”.
- Auto Restart: When enabled, the device is automatically rearmed after all input signals have been sampled and read in.
- Trigger type: “External” or “Soft”. When set to “External”, the digitizer is triggered by a 10 Hz pulser trigger which is synchronized with the Booster Ejection trigger cycle. A “Soft” trigger is used for testing and does not need an external trigger.
- Sample Rate: Number of samples per second. This is the same for rate for all input channels.

The sampled signals are read in as waveform records by the IOC. Currently, Amplitude and Phase (as I and Q) for each of the following ten signals are monitored: (a) Cavity Cell probes 1 through 5. (b) SSA Output Forward and Reverse power. (c) Circulator Input and Output, Forward and Reverse power. Figure 6 shows the User Interface for the GTR PCIe digitizer and a couple of waveforms that are sampled.

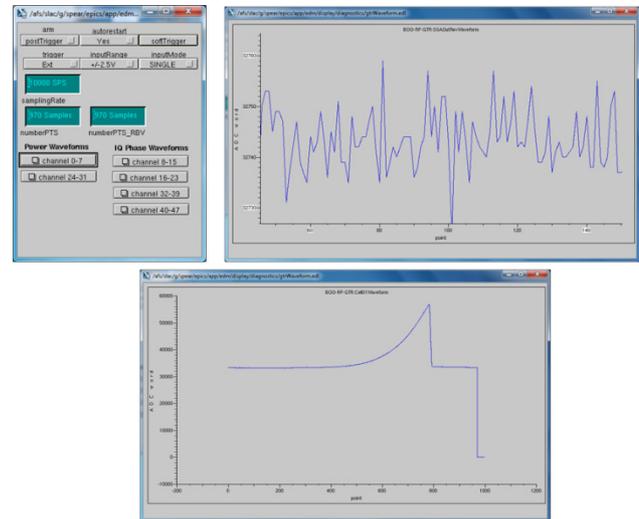


Figure 6: PCIe Digitizer GTR Controls interface.

## PLC MPS IOC CONTROLS

The Machine Protection System for the upgraded Booster RF Cavity controls comprises of Allen Bradley PLC modules from the CompactLogix family. These PLCs monitor such quantities as temperatures, vacuum, water flow, etc. and provide machine protection by fault detection and system trips.

## MPS IOC

The MPS Soft IOC runs on the Linux Server and communicates with the Allen Bradley PLC module using the EtherIP module [9]. Read back of various Booster RF scalar analog signals such as temperature, pressure, voltage, current etc. and digital Interlock statuses are provided by the IOC. The IOC provides Digital Output control for Fault Reset. Figure 7 shows the User Interface for the read back of the various temperatures.

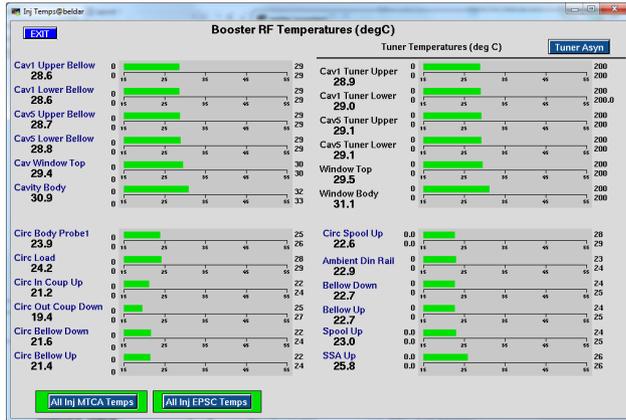


Figure 7: PLC MPS Controls interface.

## CONCLUSION

The initial phase of the commissioning of the controls for the upgraded SPEAR3 Booster RF hardware has been completed successfully. The ATCA LLRF IOC and the PLC MPS IOC will be upgraded to include more features in the near future. A slow feedback RF IOC running on the Linux Server is also planned and will be implemented during the current run. Operator EDM panels will need to be developed and deployed in production in addition to the Expert panels that are available during the commissioning period. Operator training for the new controls is also planned. The migration of the EPICS software from the existing Concurrent Versions System (CVS) repository based source control to Git based source control is also planned.

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