SLAC–PUB–8092
May 1999

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IEEE Particle Accelerator Conference (PAC 99)
New York, New York
March 29 – April 2, 1999

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Work supported by Department of Energy contract DE–AC03–76SF00515.

A SAMPLED MASTER OSCILLATOR FOR THE PEP-II B FACTORY*

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Abstract

A sampled phase-locked loop synchronizes the PEP-II B Factory rings to their SLAC Linac injector. The injection of both electrons and positrons into the separate rings and into their proper RF buckets requires phase shifting the linac RF with respect to the PEP rings. One of every three machine cycles provides the PEP ring an undisturbed reference while the other two thirds of the time the reference is unusable due to the injection scheme. The ring RF must be tunable about its nominal frequency for machine physics use. A sampled phase-locked loop handles the task of synchronizing the PEP-II RF to the linac while maintaining good phase noise. The input reference is sampled at 120 Hz and provides a ring RF signal with less than 0.1° of rms phase jitter at 476 MHz.

1 REQUIREMENTS

The PEP-II master oscillator provides the RF reference for the RF system [1], the beam feedback systems, tune monitor, and other timing needs. The design criterion for the tolerance on phase noise was the collision point offset.

During commissioning a tighter tolerance was found to be imposed by the longitudinal feedback; so the performance specification has been driven by that.

Ring RF with low phase jitter must be derived from the SLAC Linac drive signal which contains fiducials and an interferometer signal. The task is complicated by the injection scheme which shifts the phase of the linac drive signal according to the target ring and bucket of the injection bunch. The phase reference is left undisturbed for 2.8 ms of every 8.3 ms for locking the ring RF to the injection linac.

In addition to the phase shifting mentioned above, double-height, single-cycle fiducials are broadcast every 2.8 ms for machine timing use. A linac interferometer signal is superimposed on the RF for phase length stabilization. There is a 500 μs period when the bunch is in the linac when the interferometer and fiducial are not present in order to provide unmodulated RF for the linac klystrons. It is during one of every three of these periods that the PEP-II master oscillator samples the linac RF for phase locking.

The master oscillator must provide frequency tunability, smooth unlocking for tuning, and smooth locking for maintaining beam.

*Work supported by DOE contract DE-AC03-76SF00515

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2 ARCHITECTURE

The PEP-II Master Oscillator resides in the region 8 control room of the PEP-II ring. It takes linac RF as its input and produces RF fanned out for use by the RF, feedback, and timing systems, see figure 1. The designation of master oscillator is perhaps a misnomer as it actually slaves off of the linac RF.

The system consists of two second-order phase-locked loops (PLLs). The sampling first loop creates a 59.5 MHz clock with a voltage controlled crystal oscillator (VCXO). This 59.5 MHz serves as the reference for the continuous second loop which controls a voltage-controlled surface acoustic wave oscillator (SAW) running at 476 MHz. The close-in phase noise of the crystal, even after multiplication is better than the SAW oscillator's phase noise at lower frequencies.

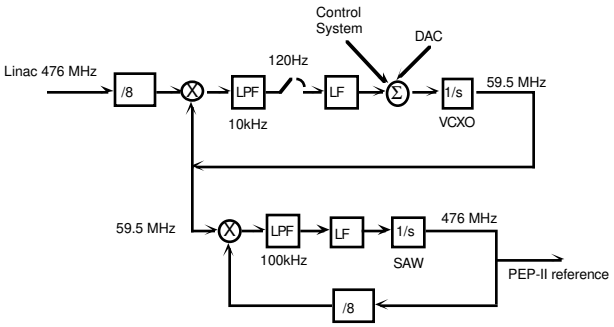

Figure 1. System Block Diagram

Most PLLs are continuous-time, closed-loop feedback systems. The nature of the PEP-II reference dictates a sampled feedback system. A low sample rate (120 Hz) restricts the available gain in the loop in order to maintain stability. The loop bandwidth must be less than the Nyquist frequency of 60 Hz. The ability to track the reference is therefore compromised. Fortunately the reference is fixed and thus only the lowest frequency behavior must be matched. The challenge is to lock with such low bandwidth and produce clean RF for the rings.

2.1 The Use of Two Loops

The loop gain in the first PLL is defined by three gain terms and the loop filter chosen. The required tuning range for machine physics and the sample rate define a frequency by which the open loop gain must be reduced to unity for stability of the sampled loop. In order to provide ±10 kHz of tuning range, the VCO selected has 60 ppm tuning sensitivity which defines the gain, Kvco (see figure 2). The digital phase/frequency detector has a gain of

0.302V/rad. The divider ratio in the feedback is settable within a range specified by the phase-locked loop chip chosen [2]. Using the notation of e.g. [3], the loop filter is designed to provide a lead-lag effect that provides phase margin to the loop.

The tuning range and sample rate require attenuation in the loop in order to maintain stability. A better method to preserve signal-to-noise quality is for the first loop to produce an intermediate frequency which is multiplied by a second phase-locked loop. In this way, no analog attenuation, excessive component values or divider ratios (which bring about additional noise) are used. The key is to produce low phase noise intermediate frequency which is multiplied, along with the phase noise, to 476 MHz by the second loop. The sample and hold operation introduces a 30° phase lag at 10 Hz, so in order to achieve adequate phase margin the loop bandwidth must be kept low.

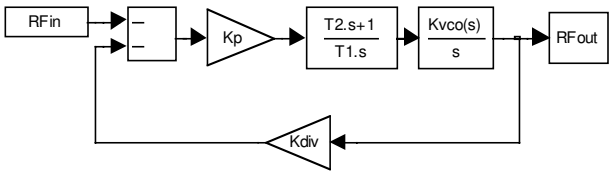

Figure 2. PLL Block Diagram

In a sampled system an antialiasing filter is used to prevent out of band information aliasing into the feedback loop. In this case the lowest bandwidth lowpass, antialiasing filter that can be used is one whose rise time must be short compared to the time span between the phase-shifted reference and the non-shifted reference to the loop. A low pass filter with 35 μs rise time is used. The rise time of a proper antialiasing filter would be nearly 6 ms and would integrate unusable reference signals along with desired time portion of the reference.

2.2 Phase Noise Apportionment

Three distinct phase noise regions contribute to the output spectrum. The first loop tracks the reference phase noise up to the extent of its bandwidth, defining the close-in phase noise of the master oscillator. The second loop tracks the first oscillator's phase noise through the second loop's bandwidth. Finally, above the second loop's bandwidth the noise is due to the final oscillator's phase noise. The SAW oscillator has a fairly low bandwidth for modulation and therefore the second loop's bandwidth is lower than would be desired from examining the optimum bandwidth based on where the first and second oscillator's phase noises cross.

The low bandwidth of the first loop means that extra care must be taken to prevent noise from reaching the first oscillator since above 60 Hz there is no disturbance rejection. Any noise imparted on the low frequencies of the first loop are dutifully reproduced by the second loop. The DC power supplies are placed in a separate chassis from the PLL circuitry for this reason. Fans for cooling are in this second chassis as well.

A signal isolation problem with the layout of the circuitry in the original design led to excess phase noise on the ring RF. A small amount of the phase-shifted reference was picked up on the clean intermediate frequency which was reproduced on the output of the second PLL. This was fixed by separating the PLL functions onto two circuit boards.

A second improvement was to use a higher frequency crystal allowing for a smaller multiplication factor leading to lower overall phase noise. The noise floor of the crystal outside the first loop's bandwidth is multiplied by the second loop within that loop's bandwidth.

2.3 Additional Features

The ring RF must be capable of running unlocked from the linac reference to allow the rings to run off nominal frequency for machine physics. The locking and unlocking procedure must be sufficiently smooth so that beam is not lost. To enable unlocking, the system has a DAC which provides the nominal voltage to the first VCO in order to produce the correct 476 MHz. The phase-locked loop provides correction about this DC value. An additional DAC is provided to allow the control system to drive the VCO in the unlocked state.

The three clocks in the system (linac reference and two VCOs) are all monitored. Should any clock fail, the loop will unlock and a flag is set in the PEP-II control system. A lock indicator is provided for the first loop. Analog signals like the first loop's raw phase error, the first loop's sampled and held phase error, and the second VCO's tuning voltage are also monitored in the control system.

3 PERFORMANCE

3.1 Jitter Analysis

A phase noise spurious sideband of low modulation index produces phase jitter according to:

$$\phi_{\mathrm{rms}}^2 = 2\mathrm{L}(\mathrm{f}) \qquad (1)$$

where L(f) is the single-sideband phase noise to carrier ratio per Hz, usually presented logarithmically in dBc/Hz [4].

The largest spur is the one at the phase shift rate which is -90 dBc/Hz. This produces only 0.0036° of phase jitter. The phase-shifted linac reference leaks onto the reference to the second PLL and leads to this spur.

It is the integrated phase noise spectral density that leads to the bulk of the phase jitter. The relation for finding the rms phase jitter for a given single-sideband spectral density is:

$$\phi^2_{\text{rms}} = \int_{f1}^{f2} 2\mathcal{L}(f)\,df \qquad (2)$$

where f1 and f2 are the starting and ending frequencies of interest, respectively.

Presently, the phase noise spectral density is <-100 dBc/Hz at 300 Hz and is lower at higher frequencies as shown in figure 3. The integration of the spectrum leads to 0.075° rms phase jitter on the RF. At 476 MHz this is 0.44 ps of timing jitter. The noise floor of the spectrum analyzer is comparable to the spectrum observed when measuring the master oscillator output. The calculation is therefore a worst case value. As the PEP-II bunch length is 1 cm or 5.7°, the rms jitter equates to about 1.3% of the bunch length.

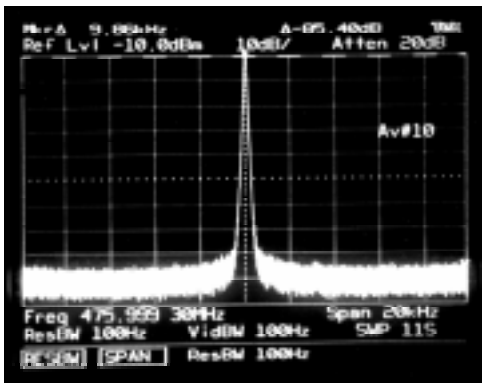

Figure 3. PEP-II RF Spectrum

The spectral density of the 59.5 MHz output is difficult to measure directly because the spectrum analyzer noise floor is higher than that of the 59.5 MHz signal. This is confirmed by noting that the 476 MHz measurement has essentially the same characteristics at the higher frequency, when it is expected to be degraded by 20*log(N), where N is 8 leading to a degradation of 18 dB. The two measured spectra are comparable, for example, at a 1 kHz offset, confirming that spectrum analyzer limitations are being observed. The spectrum is better than that of its reference since the reference is produced by multiplying a 8.5 MHz crystal to 476 MHz. The specification for the present SLAC linac crystal is -135 dBc/Hz at 1 kHz which when multiplied by 56 adds 35 dB. An imminent upgrade of the SLAC linac crystal should bring about an improvement to the PEP-II spectrum at low frequencies in the bandwidth of the first loop.

3.2 Jitter on the Beam

The rms beam motion is the integration of the product of the spectral density in Eq. 2 and the absolute value of the beam phase transfer function as shown in Eq. 3. and plotted in figure 4,

$$\phi^2_{rms} = \int_{f1}^{f2} \left| \frac{\omega_s^2}{(j2\pi f)^2 + \frac{j2\pi f\omega_s}{Q} + \omega_s^2} \right| \mathcal{L}(f)\,df \qquad (3)$$

where ω_s is the synchrotron frequency, Q is $\tau*\omega_s/2$, where τ is the radiation damping time [5].

Using this calculation with the phase noise density and the beam phase transfer function indicates that the synchrotron resonance has a slight amplification effect on the phase noise transmitted to the beam.

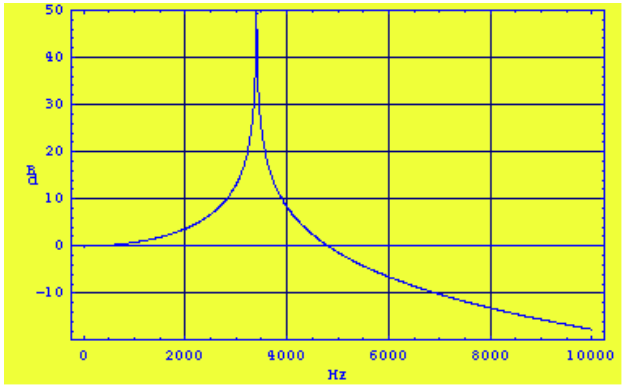

Figure 4. RF Phase to Beam Phase Response

Integrating the expression in equation (3) for the two PEP-II beams leads to 0.099° rms jitter for the LER and 0.107° for the HER.

Measurements in PEP-II before the modifications described here (circuit separation, higher frequency VCXO) indicated longitudinal beam motion of less than 0.3° in each ring. Before improvements to the layout, when the effects of the phase shifting were felt, motion was more than a degree. It is believed that the two modifications should bring about further improvement to the levels arrived at in this paper.

4 CONCLUSION

Using two phase-locked loops in succession, the PEP-II Master Oscillator provides a low jitter RF source for the RF, timing, and feedback systems.

5 REFERENCES

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