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The Readout Electronics for Silicon Tracker of the GLAST Beam Test Engineering Model

R. P. Johnson[a], T. Handa[b], V. Chen[a], H. A. Hernando[a], M. Hirayama[a], S. Kashiguine[a], W. Kröger[a], G. Meddeler[a], G. Paliaga[a], P. Poplevin[a], W. Rowe[a], H. F.-W. Sadrozinski[a], E. Spencer[a], S. Stromberg[a], A. Webster[a]

[a] SCIPP, University of California Santa Cruz, Santa Cruz, CA 95064

[b] Stanford Linear Accelerator Center, Menlo Park, CA 94025

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Abstract

The design of the Gamma-ray Large Area Space Telescope (GLAST) pair-conversion tracker is based upon single-sided silicon-strip detectors with 36 cm long strips. The electronics used to read out this system are based upon CMOS ASICs and are similar in many ways to electronics used in high energy physics experiments. However, stringent requirements on power consumption and reliability, which are required for operations in space, have lead to a unique custom design. In this paper we describe the design and construction of a fully functional prototype readout system and its performance in a beam test.

1 Introduction

The Gamma-ray Large Area Space Telescope (GLAST) is a next generation high-energy gamma-ray mission designed for observing celestial gamma-ray sources in the energy range from 20 MeV to 300 GeV with a field of view of greater than 2 steradian, which is anticipated to be launched in 2005. The Large Area Telescope (LAT) [1] on the GLAST mission is a gamma-ray pair conversion telescope that makes use of silicon-strip detector technology for the tracker-converter section [2, 3]. LAT is intended to improve sensitivity by a factor of 50 or more compared to its predecessor, the EGRET experiment on the Compton Gamma Ray Observatory [4]. That is accomplished primarily by taking advantage of silicon-strip detector technology, which provides nearly 100 % efficiency for charged particles, optimal angular resolution, very little dead time, excellent multi-track separation and self triggering capability. Silicon-strip detector technology is known to be robust, requires no consumables, such as gas, and operates at a relatively low voltage, compared with spark or drift chambers. It therefore appears to be ideally suited for space applications. All but the bottom few layers have a thin lead foil preceding the detector planes, to convert the incident gamma-ray photons into electron-positron pairs, which are subsequently tracked by the remaining detector layers to determine the photon direction. Finally, the calorimeter absorbs the electrons and thereby measures the photon energy.

The GLAST instrument design has nearly a million binary readout silicon-strip channels. Two clear limitations on operating such a system in space are the availability of power for the electronics and the difficulty of dissipating the resulting heat. Previous silicon-strip systems, designed for operation in ground-based experiments, have not needed to contend with such severe power limitations. For those reasons, a major goal of the research and development effort within the GLAST collaboration has been to design and test readout electronics that can meet the signal-to-noise requirements with minimal power dissipation.

2 GLAST Beam Test Engineering Model

The GLAST LAT consists of a 4×4 square array of nearly identical tower modules. Each tower consists of a silicon-strip tracker followed by a CsI calorimeter. The array of 16 towers is surrounded by a hermetic anti-coincidence detector (ACD). In order to validate the instrument design and the feasibility of its construction, a full-size model of one of the towers called Beam Test Engineering Model (BTEM) was built. The BTEM was tested using many electronic and mechanical aspects of GLAST, including the performance in gamma, positron and hadron beams up to 20 GeV at SLAC during two months in 1999/2000. The beam test setup is described in detail in Reference [5]. The BTEM consists of a stack of 17 trays, with a footprint of 32 cm$\times$32 cm. A prototype of the tray is pictured in Figure 1. A tray has single-sided silicon detector layers on the top and the bottom faces, with the readout electronics located on the edges. The orientation of the readout strips is the same for both sides of the detectors in a tray. Alternating trays are stacked 90° with respect to each other, such that the detectors on the bottom of one tray and the detectors on the top of the tray below form an x–y measurement pair, separated by only 2 mm. With the exception of the bottom two, each x–y pair has a thin lead converter foil located just above it. A silicon detector layer consists of five 32 cm silicon ladders. A ladder consists of 5 detectors made from 4-inch wafers(6.4 cm $\times$ 6.4 cm) or 3 detectors made from 6-inch wafers (6.4 cm $\times$ 10.7 cm). All readout strips are wire-bonded forming 32 cm long strips. Total number of ladders used in the BTEM is 130. The construction of the BTEM is described in detail in Reference [6].

The readout electronics for the BTEM tracker were designed to be as close as possible to the LAT flight instrument design. The low power, low noise amplifier-discriminator design [7] was already proven in the GLAST 1997 beam test [8]. Furthermore, in the BTEM we have also implemented the complete design for the data-acquisition aspects of the front-end electronics. The BTEM trigger consists of tracker, calorimeter, external from the beam line, and ACD veto as shown in figure 2. Tracker trigger requires three in a row of x-layers AND of associating y-layers. The trigger signal from a layer is fast-OR of 1600 channels. Calorimeter trigger is an OR of the energy deposition in each log. ACD veto signal is also an OR of each ACD tile. The signal from the beam line triggered the BTEM during the beam test, and the states of the Level-1 trigger were recorded. The self-trigger from Tracker or Calorimeter was consistent with the external beam line trigger for greater than 99% of events which generated a particle. In the following, we describe the design and testing of the front-end electronics, and a brief result of the beam test focusing on the electronics point of view, such as detection efficiency of charged particles and the noise occupancy.

3 Electronics System Requirements

The silicon strip detectors used by GLAST are single sided, with integrated AC coupling capacitors. The strip pitch has been chosen to be around 200 μm, which gives a good balance between the performance for low energy gammas, for which the angular resolution is dominated by multiple scattering, and the performance of high energy gammas, which is determined by the ratio of the strip pitch to the gap between measurement planes. The detector strip capacitance has been measured to be about 1.3 pF/cm. A 32 cm long strip in a ladder yields 42 pF of capacitance. That figure plus the expected minimum charge deposition in 400 μm thick silicon bulk determine the principal requirements for the readout pre-amplifier. The limited power levels available from solar panels, together with the necessity of transporting heat from the instrument to radiators, dictate the tracker readout electronics should not consume more than about 240 μW of power per channel.

Pulse-size analysis is not needed for GLAST, so the power restrictions naturally lead to a binary readout, with a simple single-threshold discriminator for each channel. The tracker must be self-triggering, however, so the electronics must produce a fast logical-OR of each entire detector plane with 1600 channels, to be used as input to the trigger logic. It is desired that the readout system be able to accommodate trigger rates as high as 10 kHz with minimal dead time. This necessitates clocking out of data from the chips while the amplifier inputs are active. The event trigger will probably be a simple coincidence between 6 consecutive detector planes (3 in the x view and 3 in the y view) as shown in figure 2. Assuming that the coincidence window is about 1 μs, the single-channel occupancy must be less than 10^{-4} in order to keep the noise trigger rate of the overall instrument well below the cosmic ray rate. In addition to the noise occupancy requirement, the efficiency for charged particles within the fiducial area has to be greater than 99 %. For the detectors proposed for GLAST, that roughly translates into the requirement that the equivalent noise charge not be more than about $\frac{1}{4}$ fC (1560 electrons).

The radiation exposure in the GLAST orbit will be modest compared with the environment of detectors in contemporary accelerator beams, with only about 1 kRad per year predicted. We expect to be able to demonstrate that standard CMOS processes can, with sufficient care taken in the design, withstand that level of radiation with no degradation in performance. However, it is important that redundancy be built into the readout system, to avoid the possibility of catastrophic single-point failures. Finally, the readout electronics must be designed to fit into a very narrow space along the edge of a detector plane, to minimize the dead area within the instrument.

4 The Electronics System

Two ASICs were custom designed for the tracker readout, front-end amplifier-discriminator GTFE64 chip and readout controller GTRC chip. They implement the full functionality desired for the flight instrument and satisfy the requirements on noise performance and power consumption as well as data rate. They were implemented in the HP $0.8\,\mu$m CMOS process, but they have not been space qualified. It is foreseen to use the HP $0.5\,\mu$m process in the flight, space qualified revision. The power consumption of $< 210\,\mu$W/channel has been achieved in the BTEM electronics, including all digital activity on the front-end readout board, assuming a high (12 kHz) trigger rate. In the GTFE64 chip, each channel includes a charge sensitive pre-amplifier, followed by an RC/CR shaping amplifier, a comparator, a digital mask, an 8-event deep FIFO buffer, and a latch. The pre-amplifier is AC coupled to the shaping amplifier, which has a peaking time of about $1\,\mu$s. The latches are arranged as a shift register, such that the latched data can be read out serially. In addition, there is a logical OR of the comparator outputs after the mask, to be used as a fast trigger, and there is an internal pulse generator, together with a 64-bit mask, to allow an adjustable charge to be injected into the inputs of any subset of channels.

Figure 3 illustrates the flow of data and control signals in this system, showing in particular how redundancy is implemented in order to avoid catastrophic single-point failures. The output shift register is made up of two separate registers, one that shifts from left to right and another that shifts in the opposite sense. Twenty-five chips are lined up along the edge of a detector plane and connected together to form two 1600-channel shift registers. The chain may be configured, by loading the control registers, such that it is divided between any pair of chips, with all chips to one side shifting data out in one direction while the others shift data in the opposite direction. That allows any single dead chip to be bypassed in the readout without losing data from any other chips. The fast trigger OR can also be passed to the chips on the left or the one on the right.

Simulations of on-orbit background predict an average tracker readout time for background events of only 7.3 μs, with a maximum of 203 μs. Since the front-end electronics include an 8-event FIFO buffer, with the amplifier kept alive during readout, the tracker can read out well in excess of 10 kHz with negligible dead time. All signal transmission between the controller chips and front-end chips, as well as between the controller chips and the data acquisition system, is by low-voltage balanced differential signaling (LVDS), to avoid inducing digital noise into the sensitive front-end amplifiers. In addition to buffering clock, trigger, and command signals, the GTRC chips control the readout sequence, format the data into packets of addresses of hit strips, buffer the data, and handle the readout protocol with the DAQ. The chip also calculates the time-over-threshold of the Fast-OR signal and includes it in the data stream.

Each layer of silicon-strip detectors is read out by a single hybrid, which consists of 27 VLSI chips mounted directly onto a standard 8-layer, FR4 based printed circuit board. Figure 4 shows a photograph of part of a hybrid. In the picture, five GTFE64 chips are lined up along the top with their inputs wire bonded to the Kapton circuit that carries the signals around the tray corner from the detectors. Near the right top of the connector, there is one of two redundant GTRC chips. The other GTRC chip is located at the other end of the hybrid. The hybrid is mounted on the edge of a tray as shown in the Figure 1. The high number of layers in the PC board is needed in order to implement a careful design for isolation of digital noise from the analog power and ground and to ensure a clean, low-noise flow of the small signal current through the amplifiers and, via capacitors, back to the detector bias plane. As a result, no problem with noise pickup were found during beam test running, the system exceeded the stochastic noise requirements, and we demonstrated that we can accumulate new data through the amplifiers while previous events are being read from the FIFO buffers of the GTFE64 chips. The boards were loaded with passive components and connectors by a commercial vendor, followed by testing before being loaded by the same vendor with chips and wire bonded. Testing and burn-in, for one week, of the completed modules was then done. After mounting onto a tray and wire bonding to the flex circuit, each module was fully encapsulated in a soft space-qualified silicone.

5 BTEM Tracker Test Results

Initial testing of the tracker concentrated on verifying the functionality and performance of the detectors and the electronics. This was accomplished first with noise-occupancy scans and with cosmic rays. More extensive tests have been done, making use of the beam test data. All results demonstrate that essentially 100 % efficiency is obtained within the detector fiducial volume while still satisfying the noise occupancy requirements. The results also allow extrapolating the performance to the geometry of the flight instrument (36 cm instead of 32 cm long ladders).

5.1 Efficiency

Figure 5 shows the efficiency for detecting single particle tracks in a layer as a function of the discriminator threshold setting. It was measured using 20 GeV positron beams that incident perpendicular to the silicon layers (one MIP in each event). The efficiency for each of the first three threshold values up to 1.3 fC is greater than 99.9 % for both the x and y layers. The 50 % efficiency point on the curves is at about 750 mV threshold, which should correspond to the median of the landau distribution of the signal of a MIP (about 5.7 fC). This indicates an amplifier gain of about 130 mV/fC, which is in accord with the design goal. Each 64-channel front-end readout chip has a single DAC for setting the comparator thresholds. To achieve a threshold setting on every channel that is sufficiently high above the noise but still low enough for $>$ 99 % efficiency requires good threshold uniformity across the chip. The main limitation is transistor matching in the shaping amplifier circuitry that stabilizes the amplifier output baseline. Our measurements show typically a 0.05 fC RMS variation in threshold across a chip, with a few chips having RMS variations as large as 0.12 fC compared with a nominal operating threshold of 1.3 fC. During 2 months of beam test running, all threshold DACs in the system were set the same, except for one noisy ladder (5 chips), and they never had to be readjusted.

5.2 Noise Occupancy

An important parameter in the binary readout scheme of the GLAST silicon tracker is the noise occupancy. It quantifies the noise rate of a single channel within the trigger window ($\sim$1 μs) and determines the threshold setting. The noise rate for three individual channels as a function of threshold is shown in the filled circle points in Figure 6. The curve is well described as a Gaussian of the threshold setting. The RMS noise derived from Figure 6 is the equivalent noise charge of 0.18 fC or 1100 electrons. With a strip capacitance of 1.3 pF/cm, the noise slope is thus about 22 e/pF with an offset of 140 e. At a threshold of 1.0 fC, which is far below the nominal threshold of 1.3 fC used at the beam test, the noise occupancy in a 1 μs window is below 5×10^{-5}, meeting the trigger requirements.

5.3 Self-Triggering

The tracker provides the principal trigger for the GLAST instrument. The trigger design relies upon signals from individual layers that are the logical ORs of all channels in the layer. Coincidences are formed between x–y pairs, and 3 consecutive pairs are required to fire in coincidence to make a tracker trigger. This simple scheme can work only if the noise occupancy is much less than the reciprocal of the number of channels in a layer. In the prototype tower running at nominal threshold, the noise trigger rate is negligible (a few Hz). The open square points in Figure 6 shows the firing rate of the OR of all channels in a layer. The single-plane noise rate is dominated by cosmic rays above a threshold of 1.2 fC. Self-triggering of the BTEM tracker was successfully demonstrated in the beam test.

6 Conclusions

The BTEM tracker module was completed and operated very successfully and within specifications in the SLAC beam test. The present front-end electronics design consumes less than 210 mW per channel, leaving sufficient power for the remaining data acquisition instruments. The noise level and threshold variation are small enough that we can achieve greater than 99 % detection efficiency for minimum ionizing particles passing through live detector regions, while still maintaining an acceptable noise occupancy level of 0.005 % or less. The front-end electronics are in the process of being redesigned for the 0.5 μm HP process, and a prototype of the amplifier-discriminator section has already been fabricated and tested in that process. The final design will take place after a thorough review of the specifications and existing design, and prototypes will be space qualified through radiation and environmental testing.

7 Acknowledgements

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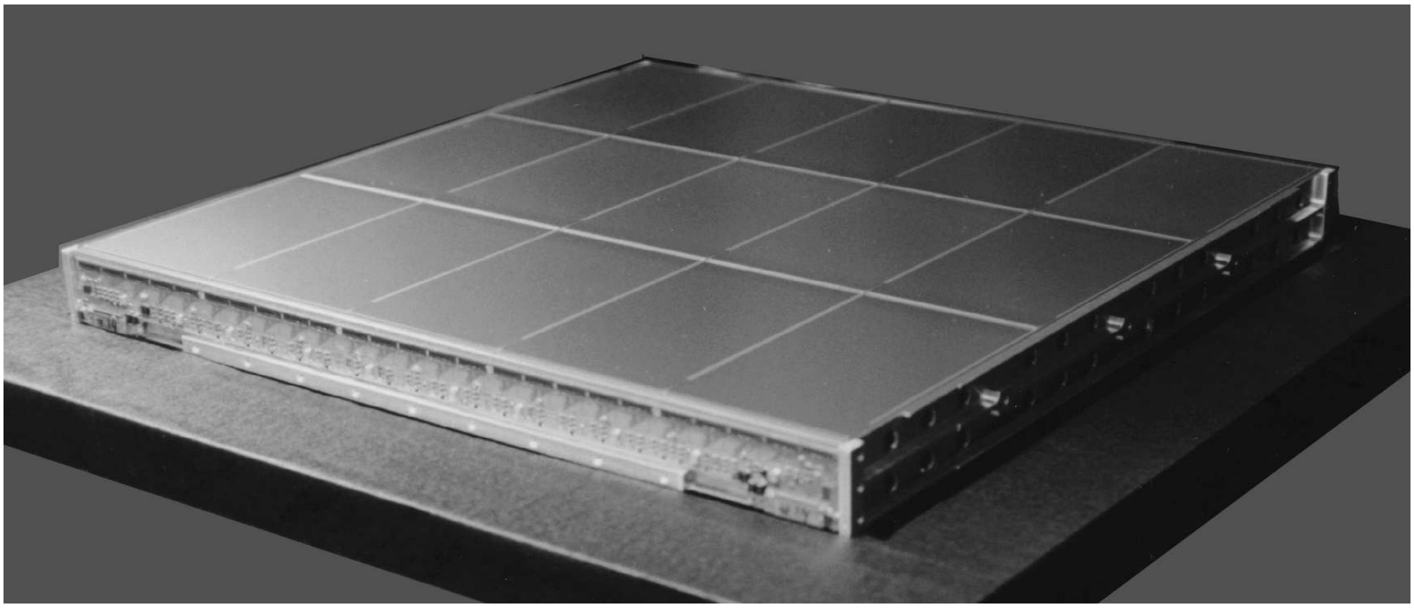

Figure 1: Photograph of one of 17 trays of the BTEM tracker. The 1600 strips in the silicon detectors on the top surface are read out by the electronics on the front edge. Not visible are a full plane of detectors on the bottom of the tray and the associated readout electronics on the rear edge.

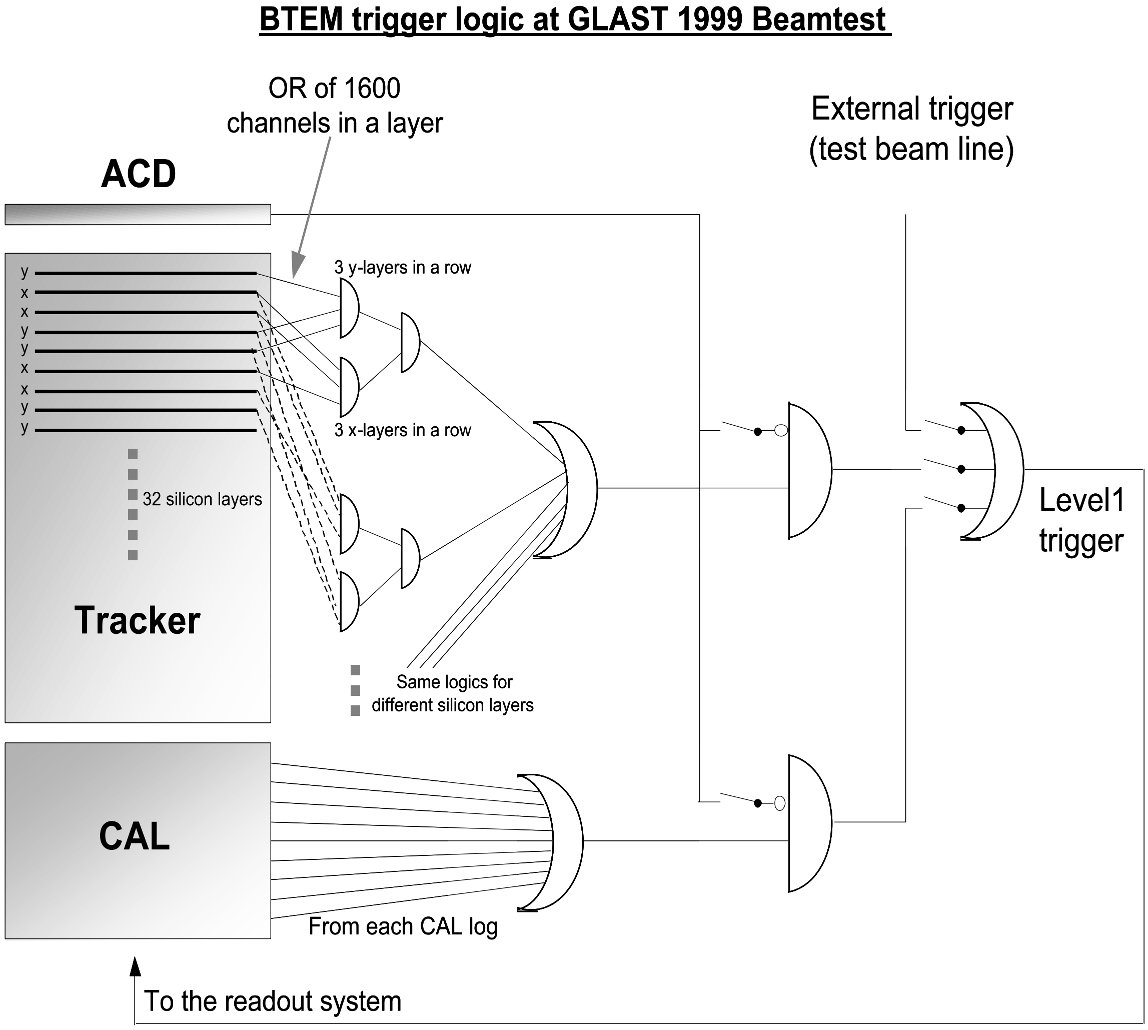

Figure 2: A schematic diagram for the level 1 trigger logic of the BTEM. It consists of tracker, calorimeter, external from the beam line, and ACD veto. Tracker trigger requires three in a row of x-layers AND of associating y-layers. The trigger signal from a layer is fast-OR of 1600 channels.

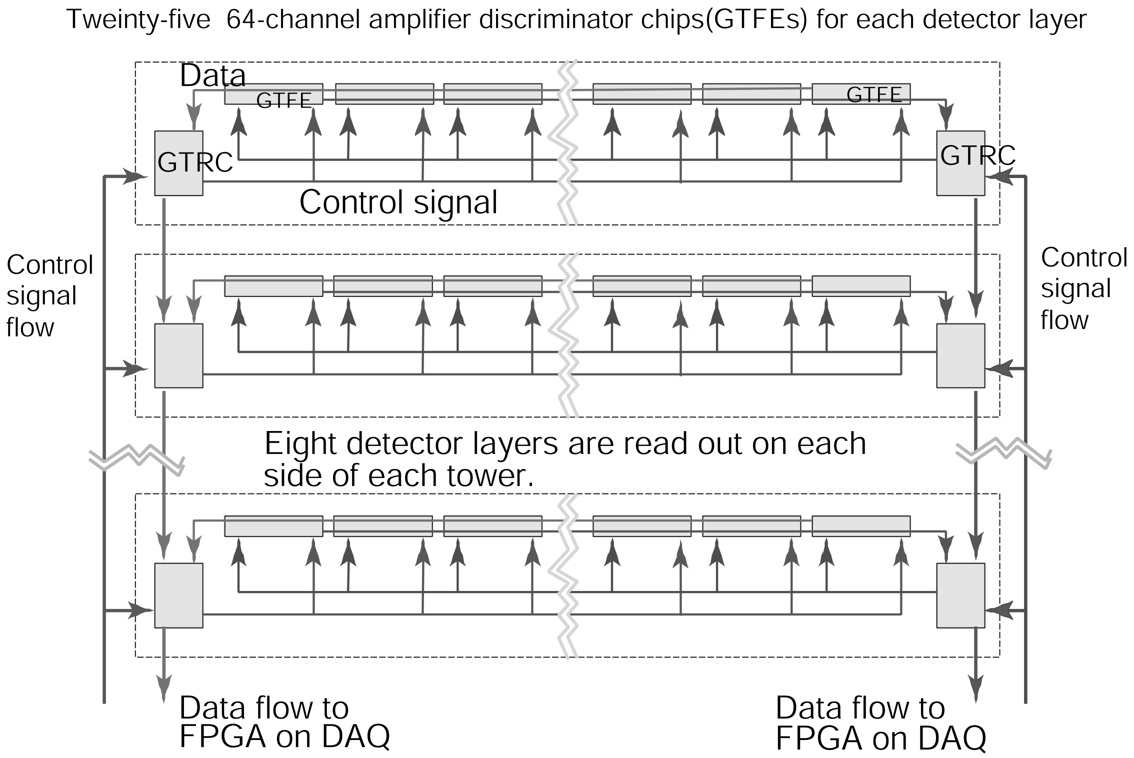

Figure 3: The readout scheme of the BTEM tracker front-end electronics, which implements the complete functionality planned for the flight system. Each readout chip can send its data to the DAQ by either of two redundant paths indicated by the arrows. Similarly, each chip can be controlled by either of two paths.

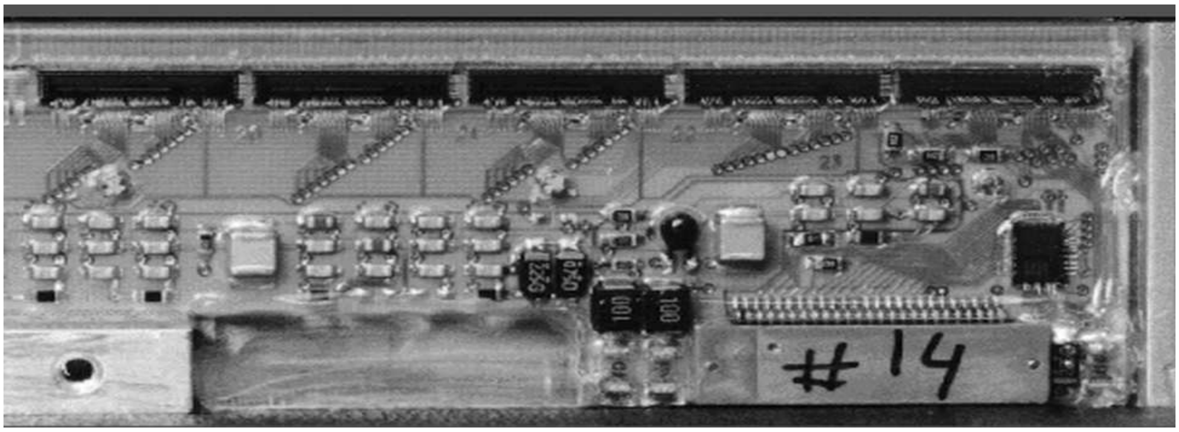

Figure 4: Photograph of the right-most 1/5 of a hybrid, shown mounted on the side of a BTEM tray.

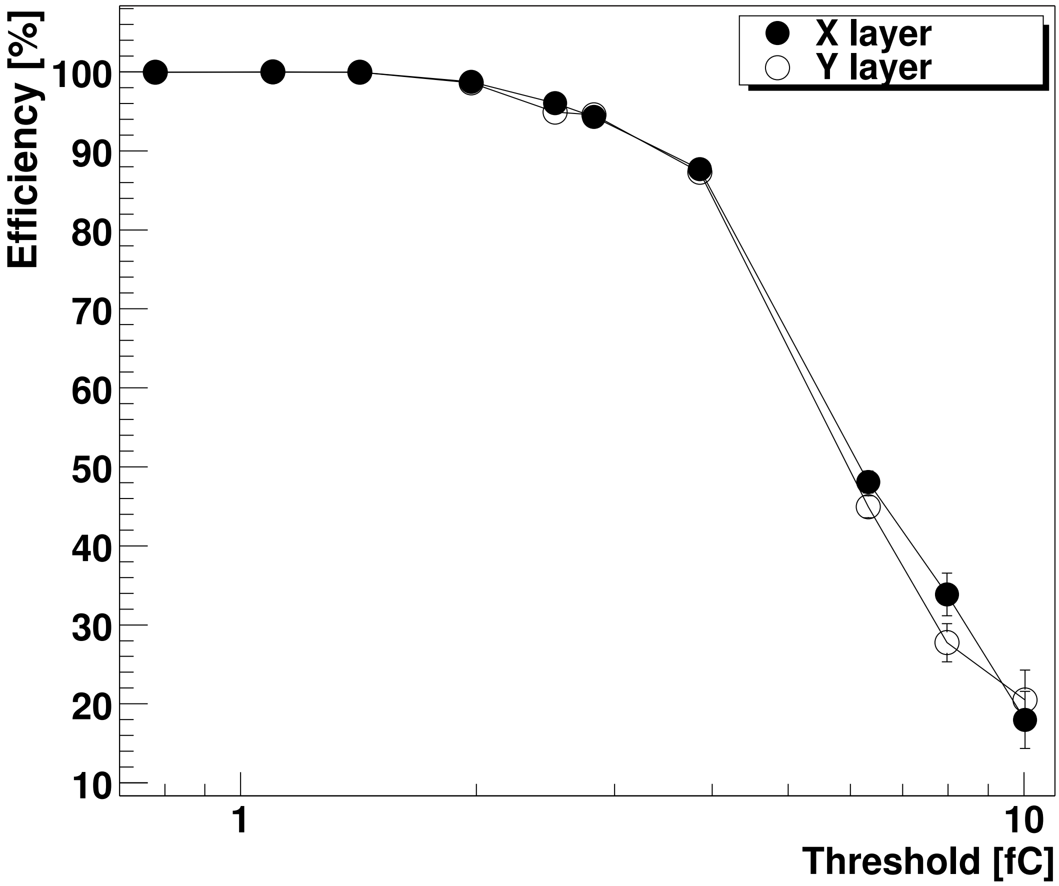

Figure 5: The efficiency versus threshold in the 10 th layer from the bottom, measured during the beam test from single 20 GeV positron tracks at normal incidence, which is perpendicular to the silicon layers. The nominal threshold for beam test running was 1.3 fC.

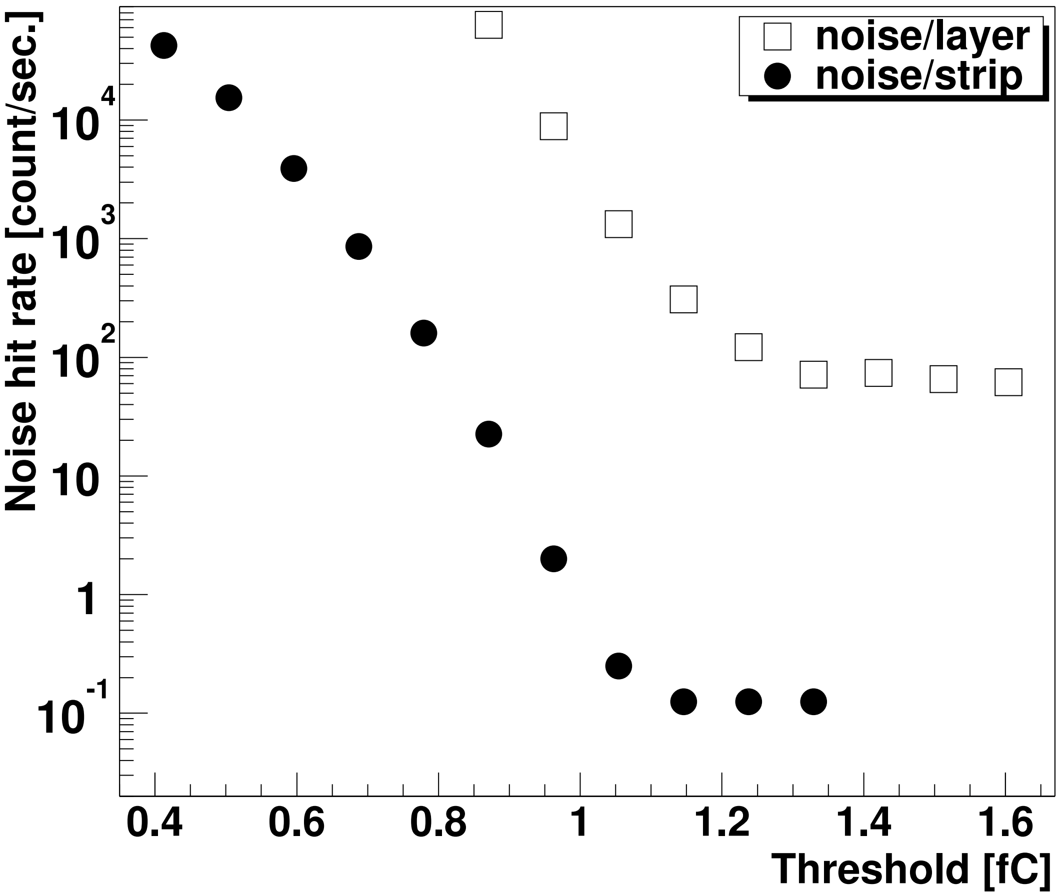

Figure 6: Noise rate as a function of the threshold. The filled circle points are from an individual channel. The open square points are from the OR of 1600 channels in a layer. The individual channel points can be fitted to a Gaussian with a noise RMS of 0.18 fC or 1100 electrons. Note that the threshold was set at 1.3 fC during the beam test.