Diborane Electrode Response in 3D Silicon Sensors for the CMS and ATLAS Experiments

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ABSTRACT

Diborane Electrode Response in 3D Silicon Sensors for the CMS and ATLAS Experiments. EMILY R. BROWN (Reed College, Portland, OR 97202) CHRIS KENNEY (Particle Physics and Astrophysics Elec. and SW Eng. Dept., Stanford Linear Accelerator Center, Menlo Park, CA 94025)

Unusually high leakage currents have been measured in test wafers produced by the manufacturer SINTEF containing 3D pixel silicon sensor chips designed for the ATLAS (A Toroidal LHC ApparatuS) and CMS (Compact Muon Solenoid) experiments. Previous data has shown the CMS chips as having a lower leakage current after processing than ATLAS chips. Some theories behind the cause of the leakage currents include the dicing process and the usage of copper in bump bonding, and with differences in packaging and handling between the ATLAS and CMS chips causing the disparity between the two. Data taken at SLAC from a SINTEF wafer with electrodes doped with diborane and filled with polysilicon, before dicing, and with indium bumps added contradicts this past data, as ATLAS chips showed a lower leakage current than CMS chips. It also argues against copper in bump bonding and the dicing process as main causes of leakage current as neither were involved on this wafer. However, they still display an extremely high leakage current, with the source mostly unknown.

INTRODUCTION

Semiconductor Theory

The basic theory of semiconductor detectors centers around the small ionization current caused when a charged particle loses part of its energy through elastic collisions with electrons as it travels through a material [1]. Most semiconductor detectors consist of a silicon crystal wafer doped and reverse biased, which makes it a diode. Doping refers to the addition of an impurity to the pure semiconducting material in order to change its electrical properties. For silicon, adding a column V impurity, such as phosphorus, donates an electron to the semiconductor, creating an n-type semiconductor. Adding a column III impurity, such as boron, creates an excess hole, or lack of an electron, forming a p-type semiconductor [2]. Various patterns of doping are used in detectors for different purposes and to various degrees of effectiveness. For a more detailed explanation, see textbooks by Sze, Grove or Lutz.

Originally, semiconductors were doped only on the surface of the silicon, or using planar technology. In contrast, doping of the detectors in ATLAS and those used in many other situations penetrates into the substrate of the silicon. Electrodes are etched, doped and filled in various patterns which determine maximum drift and depletion distances. Figure 1.1 displays an ionizing particle traveling through a planar detector, while Figure 1.2 is a diagram of 3D electrodes. Advantages of three-dimensional (3D) electrodes include a greater resistivity to radiation damage, they read out faster and that the shape of the detector is not restricted to a square [3]. However, because the 3D etching process essentially turns the silicon into a sponge-like shape, it is more difficult to keep clean as there are more places for contaminants to settle. The manufacturing process itself is also more difficult than those of planar technologies.

ATLAS

ATLAS, or A Toroidal LHC Apparatus, is one of the six particle detectors on the Large

Hadron Collider (LHC) at CERN in Geneva. It is designed to be a general-purpose detector, combining an inner detector to precisely record position of particles with outer layers of calorimeters, toroids and muon spectrometers to measure momentum and energy of particles resulting from a proton-proton collision [Fig. 2.1] [4]. The goals of the experiment range from completing the standard model to looking for evidence of dark matter, the Higgs boson, and supersymmetry, amongst other theories. The high energy capacity of the LHC (14 TeV) provides a unique opportunity to study never-before-seen physical phenomena, and the ATLAS experiment strives to gather as much information from the collisions in the LHC as is currently possible.

The very innermost layer of ATLAS is comprised of semiconducting silicon pixel detectors which precisely record the positions and vertices of charged particles resulting from the collision [Fig. 2.2]. These detectors need to be as precise as possible in order to detect potential particle decays by showing particle paths not originating from the position of the original collision. These decays can happen in a scale of nanometers, so reducing the noise to signal ratio is incredibly important.

The barrel and end disks of the pixel detector are made up of 1744 modules consisting of a silicon $n+\text{ on } n$ sensor, 16 front end (FE) chips, and a module control chip (MCC) [Fig. 2.3]. The silicon sensor is what detects all of the particles that come in contact with the detector, and every pixel of the sensor is connected to a pixel on the front-end chip. The front end chip is a 3-D silicon chip that is a charge sensitive amplifier with leakage current subtraction, signal shaping, a programmable threshold discriminator, and Time over Threshold (ToT), i.e., an 8 bit measurement for charge amplitude. After the FE chip initially sifts through the data, it is sent to the MCC which combines the individual events and distributes trigger and command signals. The silicon sensor is glued to a kapton-flex hybrid and bump bonded to the FE chip, and the MCC and FE chips are connected through pigtail connectors [5, 6]

CMS

CMS, or the Compact Muon Solenoid, is another general purpose detector on the LHC with similar experimental goals as ATLAS. It consists of a large superconducting solenoid with calorimeters and muon chambers, and an inner core consisting of pixel detectors [Fig. 3.1] [7]. It also has three barrel layers of modules but has only two end-cap disks with modules tilted at 20 degrees to form a fan shape, in contrast to the ATLAS detector which has three flat end cap disks on each end [Fig. 3.2]. This layout is used to induce charge sharing so that the drift direction is not parallel to the magnetic field [8].

The CMS modules are also very similar to those of ATLAS, consisting of an n+ on n silicon sensor bump bonded to 3-D silicon readout chips (ROCs) glued to a high-density interconnect (HDI) which holds the Token Bit Manager Chip (TBM). The ROCs have similar functions to the FE chips on the ATLAS modules, and the TBMs control the readout of the ROCs, again similar to the MCCs on ATLAS. The main differences between the two experiments are in the designs of each of the components and in their size. For example, the ROCs on CMS have 80 x 52 pixels, and a pixel size of 100 μ m x 150 μ m, while the FE chips on ATLAS have 160 x 18 pixels and a pixel size of 50 μ m x 400 μ m. Both have a resolution of 10 μ m in the r ϕ coordinate system, but the chip design clearly differs [8, 9]. The two experiments are intended to complement each other in their searches for physical phenomena.

SINTEF Wafer Problems

Wafers made at SINTEF in Norway have been found to have an extremely high leakage current for an unknown reason. The leakage current is large enough to occupy most and sometimes all of the dynamic range of the detector. The dynamic range is the maximum signal that the detector can handle, so if the signal is occupied by leakage current, the detector will not be able to sense any signal from particles. High leakage currents in the detector also cause it to draw a great deal of power, which should be reduced to save operating costs. In an effort to understand this, both ATLAS and CMS chips made at SINTEF have been tested at various stages in the manufacturing process. The CMS chips have been showing significantly less leakage current than the ATLAS chips, so this has led some to theorize that differences in the packaging and handling or the intrinsic geometry of the two have caused this disparity. Figures 4.1 and 4.2 show some past data on the ATLAS and CMS chips taken after bumps had been added but before the chips were diced.

MATERIALS AND METHODS

In order to add some insight into the problem, a wafer from SINTEF sent to SLAC that had only one edge cut and indium bumps added was tested. Voltage probes with an optical microscope were used to measure the leakage current in the different chip designs on different areas of the chips. The areas tested on each chip differs and a bias voltage of 10-50V in intervals of 10 was used. The wafer was tested at roughly room temperature in a non-clean environment.

Types of Chips on SINTEF Wafer [Fig. 5.1]

- "Baby ATLAS" These are small versions of the sensors that match the FEI3 chips, the front end chips currently in the ATLAS detector, created to study their behavior in smaller sizes. These range from having 1 to 5 (1E-5E) columns per pixel, and all of the pixels are connected together. They are located mainly along the edges of the top half of the wafer. The leakage current between the active edges and the chip's test pad was tested [Fig. 5.2].
- *•* FEI3 These match the FE chips currently in the ATLAS detector, which have a range of 1E-5E. They are located on the bottom half of the wafer. The leakage current between the active edge and the top right, center and bottom right pixels was tested by making contact with the voltage probe and the indium bump for that pixel.
- FEI4 These are larger versions of the FEI3s, possibly to be incorporated into the next ATLAS upgrade, both of which are 2E. They are the two largest chips in the center of the top half of the wafer. The leakage currents between the top right pixel, the center pixel and the bottom right pixel and the active edge were tested.
- CMS The current sensors in the CMS experiment which are either 2E or 4E types. They are located on the right side of the top half of the wafer. Again, the leakage current between the top right and bottom right pixels and the active edge was tested. A second set of data on the leakage current between the edge, top right, center and bottom right pixels was taken.

RESULTS

Baby ATLAS

Table 1.1 shows the total number of each kind of chip and the number and percent that broke down. The chips with the higher numbers of electrodes broke down more frequently than the others. However, this could be because those were most frequently along the edges of the wafer and many appeared to be damaged.

Table 1.2 and Figure 6 show the average leakage current by the number of electrodes per pixel. As the number of electrodes per pixel increases, so does the leakage current. The leakage current on almost all of the chips fluctuated widely, with some decreasing in current by about 30 nA per minute.

FEI3

Table 2.1 shows the number of each kind of chip on the wafer and the number and percent that broke down. Only two FEI3s broke down, possibly due to damage as one was along the sliced edge.

Table 2.2 and Figure 7 display the average leakage current by the number of electrodes

per pixel. Once more, we see an increasing leakage current with an increasing number of electrodes per pixel. The 4Es on this chip were consistently unstable at higher voltages with some decreasing by about 10 to 30 nA per minute at 50 V. The area and number of pixels measured with the technique of contacting the voltage probe with an indium bump is unclear, so it is difficult to compare these measurements to the those on the "Baby ATLAS" chips, the FEI4s and the CMS chips, but a similarity in behavior with the CMS chips will be assumed.

FEI4

Only two FEI4 chips were on the wafer tested, and neither broke down. However, the bottom right pixel of the FEI4 on the top had an extremely high leakage current which showed a more exponential shape. The bottom right pixel of that chip also had a rapidly fluctuating current, that differed around 10 nA. Comparing the leakage current measurements of these chips is difficult, as it is unclear how many pixels were measured. Table 3.2 and Figure 8 shows the leakage currents of the two chips at each of the pixels measured.

CMS

Table 4.1 shows the number of CMS chips on the wafer of each type as well as the number and percent that broke down. Only one CMS chip broke down, which could have also been due to damage, as the chip was along the top edge.

Table 4.2 and Figure 9 display the average leakage currents for the chips by number of electrodes per pixel. Figure 9 separates the data by which pixel the data was taken from. The top right pixels of the 2E chips all showed a rapidly increasing leakage current with an exponential shape, while the data from the other pixels on all of the other chips kept a much lower leakage current with a more linear shape. The 4Es also were unstable at higher voltages, decreasing in current from 10 to 40 nA per minute at 50 V.

DISCUSSION AND CONCLUSIONS

Discussion

FEI3 vs. FEI4

Figure 10 shows the average leakage current over the three points taken on the chip of the 2E FEI3s and the two FEI4s. The bottom right pixel of the top FEI4 was not included as it showed break down level leakage current while the bottom right pixel of the other did not. The FEI4s had about 3 times as more leakage current. However, it is difficult to know how many pixels the data includes so because the FEI4 pixels are smaller than those on the FEI3s; the data taken could be including more pixels on the FEI4s than the FEI3s. Additionally, a statistics issue needs to be taken into account since the sampling of FEI4s was much smaller than that of the FEI3s.

FEI3 vs. CMS

Figures 11 and 12 show the average leakage current over the three points taken on the chip of the FEI3s and the CMS chips separated by the number of electrodes per pixel. On both chip types, the FEI3s showed a lower leakage current than the CMS chips, contradicting past data. Again, there could be an issue with sample size because there were about twice as much FEI3s than CMS chips, so the CMS data could be more skewed. The chips that broke down of either type were not included in the averages.

Conclusion

The SINTEF wafer shows completely different behavior than the others, as the FEI3s actually performed better than the CMS chips. Therefore this data argues against the differences in packaging and handling or the intrinsic geometry of the two as a cause in the disparity between the leakage currents of the chips. Even though the leakage current in the FEI3s overall is lower, the current is still significant enough to cause problems. As this wafer was not diced, nor had it any copper added for bump bonding, this data argues against the dicing and bump bonding as causes for leakage curent.

To compliment this information, more data will be taken on the efficiency of the individual electrodes of the ATLAS and CMS chips on this wafer. The electrodes will be shot perpendicularly with a laser to test the efficiency across the width of the electrode. A mask with pinholes has been made to focus the laser to a beam smaller than the width of an electrode in order to properly scan it. This will provide more information on whether something in the electrodes, such as the polysilicon filling, is contributing to the leakage current or if there is another cause to be found. It will also reveal whether the diborane doping method and the new polysilicon filling has increased the electrode efficiency as expected. Thus, the cause of these leakage currents on the wafers from SINTEF has yet to be definitively found.

FIGURES AND TABLES

Figures

Fig. 1.2 - Three-dimensional view of electrodes in a 3-D detector [10]

Fig. 3.2 - CMS inner detector [7]

Fig. 4.1 - FEI3 data taken at SINTEF with bump-bonding [13]

Fig. 4.2 - CMS data taken by Purdue and Fermilab [13]

Fig. 5.1 - SINTEF Test Wafer

Fig. 6 -"Baby ATLAS" Average Leakage Current

Fig. 7 - FEI3 Average Leakage Current

Fig. 8 - FEI4 Leakage Current

Fig. 9 - CMS Average Leakage Current

Fig. 12 - FEI3 vs. CMS 4E

Tables

Table 1.2 - "Baby ATLAS" Average Leakage Current (nA) Separated by $\#$ of Electrodes

$\#$ of Columns 10 V 20 V			30 V	40 V	50 V
1E	58.182	154	337.455	626.364	995.455
2E	130.125 282		575.375	1059.5	1748.75
3E	179	371.2	714.5	1113.5	1821
4E	220	462.1	828.1	1226.9	1936
5Е	351.714	796.571	1427.143	2332.857	3672.857

Table 2.1 - FEI3 Table of $\%$ Break Down

$\#$ of Columns 10 V 20 V 30 V				40 V	50 V
1E	28.333	32.333	35.667	38.167	41.167
2E	76.033	93.1	105.1	- 115.567	127.267
3E	169.333			188.444 208.056 232.389 257.5	
4E				371.467 475.633 568.233 696.033 734.348	
5E	614	748.833		839.333 913.667	977.5

Table 2.2 - FEI3 Average Leakage Current (nA) Separated by $\#$ of Electrodes

Table 3.1 - FEI4 Leakage Current (nA) On Different Areas of Chip

	Die # Test Pixel 10 V 20 V 30 V 40 V 50 V					
126	TR	170		212 255	302	354
126	\overline{C}	317		362 409	451	485
126	BR.	165		227 433 834		1440
127	TR.	154	178 206		237 271	
127	C	309		361 415	462	499
127	BR.	143	170	-203	244	294

Table 4.1 - CMS Table of $\%$ Break Down

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