Building a Better Capacitor with Thin-Film Atomic Layer Deposition Processing

SLAC National Accelerator Laboratory, 2575 Sand Hill Road, Menlo Park, CA 94025

Christopher Pike, North Seattle College

TID AIR Sensors Direcorate, SLAC National Accelerator Laboratory

Abstract

The goal of this research is to determine procedures for creating ultra-high capacity supercapacitors by using nanofabrication techniques and high k-value dielectrics. One way to potentially solve the problem of climate change is to switch the source of energy to a source that doesn't release many tons of greenhouse gases, gases which cause global warming, into the Earth's atmosphere. These trap in more heat from the Sun's solar energy and cause global temperatures to rise. Atomic layer deposition will be used to create a uniform thin-film of dielectric to greatly enhance the abilities of our capacitors and will build them on the nanoscale.

Introduction

The goal of this research is to determine procedures for creating ultra-high capacity supercapacitors by using nanofabrication techniques and high k-value dielectrics. With man-made climate change becoming more and more of a hot-button political issue, more research and public funding have been devoted to the human issues this problem causes. A recent report states that pollution in China is causing 1.6 million deaths a year. This is a huge loss for society and reduces a country's economic output by causing more sick days. [1]

The majority of this pollution is airborne particulate matter is caused from burning coal and other fossil fuels to provide the country with a growing thirst for more electrical power. As the world becomes more populous and more people get connected to technology this need for power will continue to grow across all countries. So the need to switch to a more sustainable way of supplying our future societies with power is becoming a necessity if we continue on the path we're currently on.

One way to potentially solve the problem of climate change is to switch the source of energy to a source that doesn't release many tons of greenhouse gases, gases which cause global warming, into the Earth's atmosphere. These trap in more heat from the Sun's solar energy and cause global temperatures to rise.

A proposed solution is through the use of solar panels to collect the Sun's energy and convert it directly into electricity. [2] This provides a source of electricity that doesn't

release greenhouse gases as part of the power generation step and is becoming more popular and is being places on many residential houses across the United States of America. [3].

The downside to solar energy is that it cannot be produced continually throughout the entire day and night. Luckily electricity is being created during the peak power times of the day where electricity is used to head homes, commercial buildings, and power largescale economic factories. [4] But there is still a need to either supplement that energy with some form of electricity that can be created at night or for an economical way to store large amounts of electricity between the times where energy is actively being created.

This solution directly leads into the impetus that started this research, to build a better capacitor to be able to store vast amounts of energy for society in an economic and

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scalable way. The end goal was to be able to create a capacitor and test different recipes for how well they acted as a capacitor. However, there were some difficulties that had to be resolved and it took time to truly understand the various characterization machines to get them to be able to create the devices I wanted them to create and at the proper magnitudes.

Other works in the literature were creating devices that were about one order of magnitude thicker than and our final devices will end up being once a successful recipe has been found.

Technical Approach, Impact, and Accomplishments

Equation 1 is the capacitance equation for parallel place capacitors and it is what we're basing our methods on.

$$C = \frac{k\varepsilon A}{d}$$

Equation 1 Equation for parallel plate capacitors.

Epsilon is a universal contend and so it will not be taken into consideration when thinking about design parameters. Capacitance is directly proportional to the k-value of the insulating layer and the area between the two conducting places. The thickness of the insulating material is d. Thus, we want a capacitor that is very thing, but still has a large surface area. The emerging technology that vastly increases surface area for a given volume is nanotechnology and so it will be what we'll use to create our devices. Silicon will be the chosen substrate because it is widely available and it is well understood how to fabricate devices onto it.

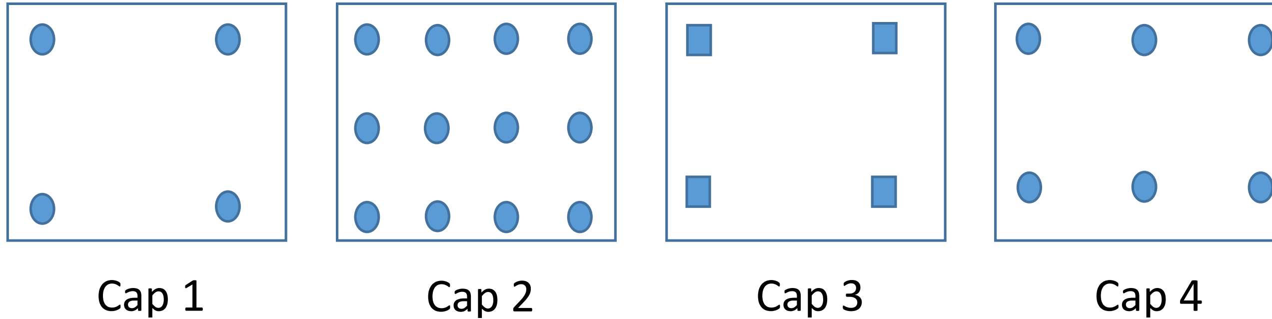


Figure 1 Mask design used for photolithography.

Hafnium oxide has been a dielectric that has been receiving a lot of attention from researchers in the silicon device industry. [5] It has a higher k-value than aluminum oxide and silicon oxide, two very common dielectrics that are already used in industry and research while still providing for low leakage currents and high breakdown voltages.

Hafnium oxide is also well characterized when fabricating through the ALD process. It deposits about 1 A/cycle, so it allows for nearly perfect for dielectric thickness.

To increase the surface area of our parallel plate capacitor we will be introducing surface features on our silicon wafer before depositing out Metal-Insulator-Metal (MIM) capacitor on top. Figure 1 shows the mask design used for the shaping of our silicon wafers.

These designs were used to pattern the photoresist and a blank silicon wafer which would then be subjected to SF_6 reactive ion etching to create through a standard Bosch

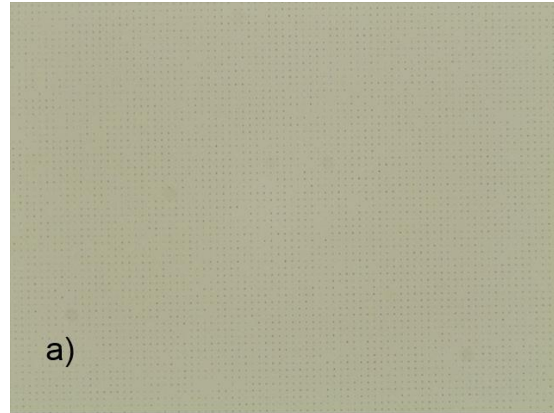
process. This includes two alternating steps, one that etches down into the silicon, and a second step, called the passivation step, that coats the side wall of the feature with a thin protective layer. This makes the etch anisotropic and allows for making features with large aspect rations. This work will aim for about a 20:1 aspect ratio.

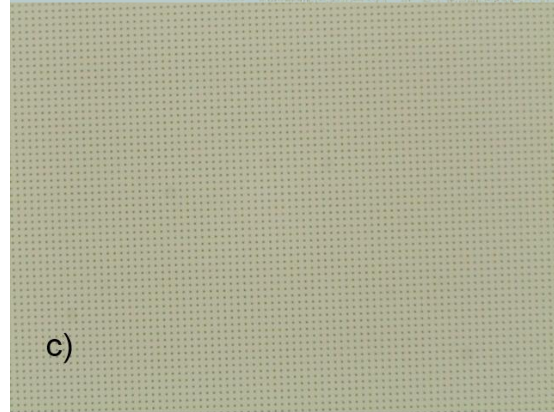
After etching, the silicon wafer will have many cylindrical holes in the area where each capacitor is to be made. This increases the surface area by many orders of magnitude, and thus it also increases the capacitance by the same value.

For the first experiment, each MIM layer will use the exact same recipe as each other and the only variable will be the number of features that are embedded into each capacitor. Each features size is .5 microns and is either the diameter or the length and width of feature, depending on what geometric shape it is. Cap 1 and Cap 2 have a pitch of 4 micron, Cap 2 has a 1 micron pitch, and Cap 2 has a 2 micron pitch.

Figure 2 shows what our results look like after a 20 minute etch.

Cap 2, with a feature size of .5 micron and a pitch of 1 micron, only has a .5 micron gap between each feature. Due to this small size there is a weird gradient where very large straight lines can be seen on a long-term scale. Further research will have to be done in order to determine the reasoning being this feature. This pattern is consistent across all wafers and occurs on each design within each individual wafer as well.





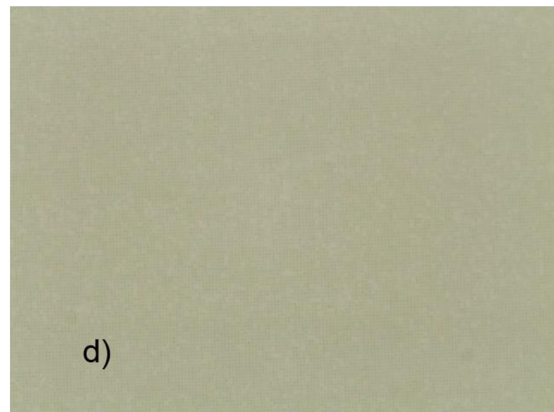


Figure 2 After 20 minutes of reactive ion etching. A) Shows surface of Cap 1. B) Shows surface of Cap 2. C) Shows surface of Cap 3 D) Shows surface of cap 4.

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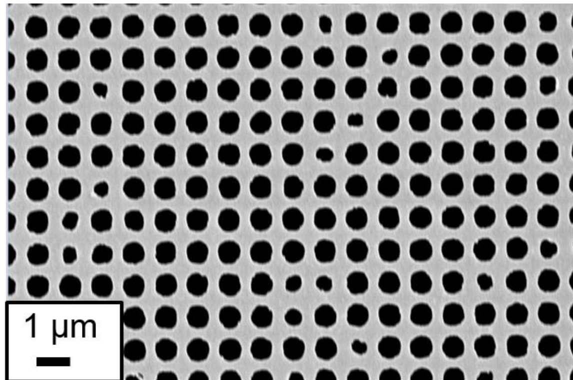
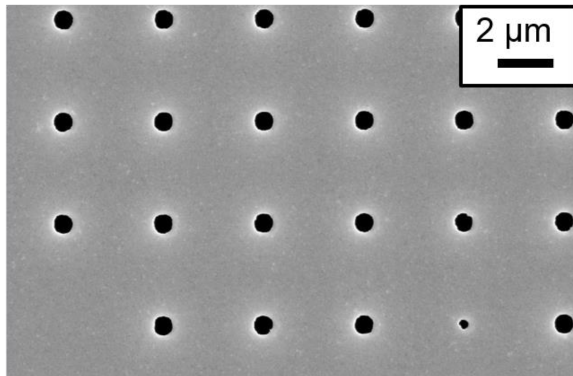
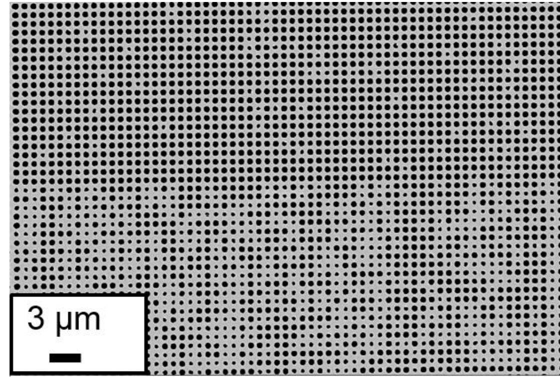
Using a scanning electron microscope we will be able to determine more information about our features.







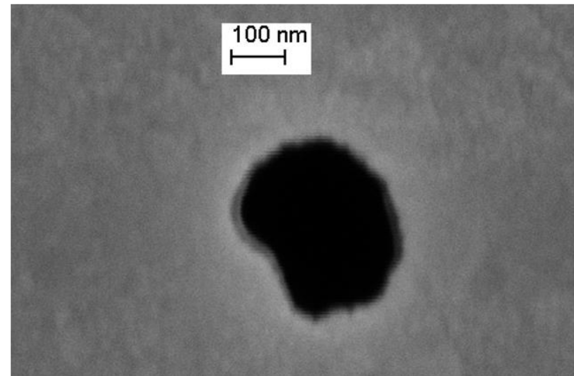


Figure 3 SEM imaging. .

Figure 3 shows that depending upon where the feature is that the range is typically between 500-1000 nm. Cap 3 shows the best uniformity.

Conclusions

The square design created circular features, which was as expected. The feature size of the square corners was too small for both the exposure step of the photolithography process as well as the etching step. What was surprising was how that small difference made such a huge difference in the resulting feature. When comparing the square design to the circle design of the same dimension and pitch, the square design created nearly perfect and consistent holes in the silicon.

The 1 micron pitch design was too much for one of the steps to handle and created a gradient of different hole sizes across the capacitor area.

Future Work

Further work must be put into determining why the square feature resulted in a drastically different result. The other anomaly that needs to be explain in further experiments is what caused the gradient in the second capacitor. Once these issues are resolved, more fine-tuning of the recipes and processes can move forward.

There are still so many parameters that can be adjusted and tweaked to continue this work. The next step is to build a functioning capacitor and then to make small changes to the insulator. How big of a difference does changing the thickness from 1 nm to .5 nm make? Theoretically we know the results, but it is still unknown whether the ALD process can create electrically stable thin-films with no pinholes that will affect how the capacitor works.

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I will be transferring to the University of Washington in the fall quarter to pursue an electrical engineering degree and will continue doing research related to meeting the future electrical needs of our society.