Design and Evaluation of a Clock Multiplexing Circuit for the SSRL Booster Accelerator Timing System

Million Araya†
August 21, 2015
Seattle Central Community College, Seattle, WA
CCI Program, SLAC National Accelerator Laboratory

SPEAR3 is a 234 m circular storage ring at SLAC's synchrotron radiation facility (SSRL) in which a 3 GeV electron beam is stored for user access. Typically the electron beam decays with a time constant of approximately 10hr due to electron lose. In order to replenish the lost electrons, a booster synchrotron is used to accelerate fresh electrons up to 3GeV for injection into SPEAR3. In order to maintain a constant electron beam current of 500mA, the injection process occurs at 5 minute intervals. At these times the booster synchrotron accelerates electrons for injection at a 10Hz rate. A 10Hz 'injection ready' clock pulse train is generated when the booster synchrotron is operating. Between injection intervals-where the booster is not running and hence the 10 Hz 'injection ready' signal is not present-a 10Hz clock is derived from the power line supplied by Pacific Gas and Electric (PG&E) to keep track of the injection timing. For this project I constructed a multiplexing circuit to 'switch' between the booster synchrotron 'injection ready' clock signal and PG&E based clock signal. The circuit uses digital IC components and is capable of making glitch-free transitions between the two clocks. This report details construction of a prototype multiplexing circuit including test results and suggests improvement opportunities for the final design.

I. Introduction

The ultimate purpose of a synchrotron radiation facility is to generate stable, high-power beams of light spanning from the Infrared to x-ray portion of the electromagnetic spectrum. These beams of light can then be used by the experimental community to characterize a wide range of physical and biological material samples. This is achieved by accelerating electrons to nearly the speed of light using a high-power radio frequency source - hence the name 'synchrotron' - and having the electrons constantly change direction along the arc of a circular accelerator using strong magnetic fields. As the electrons circulate around the accelerator they emit photons or 'synchrotron radiation' which is then transported and focused in a number of x-ray photon beam lines for use by experimental scientists. In the process, some of the electrons in the beam collide with gas particles in the beam chamber or with each other as they move around the ring and breakout from the beam. As a result, the beam loses electrons that need to be replenished for the system to be able to generate a continuous source of synchrotron radiation. Replenishment is done by injecting new electrons into the storage ring every 5 minutes from a 'booster' synchrotron. Among other things, the booster synchrotron consists of an electron gun, linear accelerator, and storage ring in which the electrons are accelerated until they acquire the desired level of energy.

SLAC National Accelerator Laboratory, 2575 Sand Hill Road, Menlo Park, CA 94025

† This material is based upon work supported by the U.S. Department of Energy, Office of Science, Office of Workforce Development for Teachers and Scientists (WDTS) under the Community College Internship (CCI) program, under Contract No. DE-AC02-76SF00515.

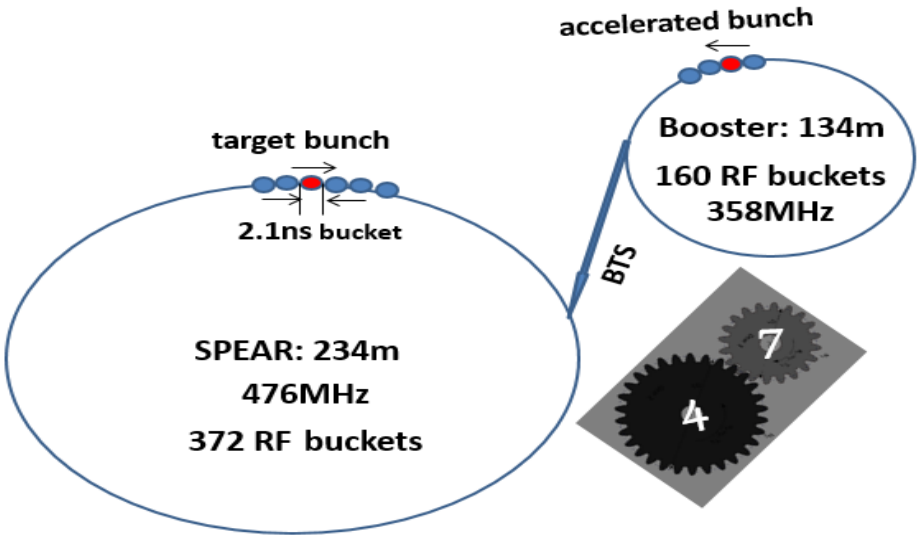


Figure 1: Schematic of SPEAR3 and the Booster Synchrotron

Figure 1 shows the main SSRL synchrotron 'SPEAR3' which stores the electron beam for x-ray production along with the booster. The beam in SPEAR3 consists of about 300 electron bunches revolving around the ring at a relative spacing of 2.1ns defined by the radio frequency system. Each time a new injection of electrons into SPEAR3 is required, a fresh bunch is first injected into the booster to be accelerated until it gains the desired level of energy of 3GeV. Next, it is transferred into the storage ring to reinforce a specific target electron bunch. This needs high level of coordination and therefore a complex timing circuit operating at the sub-nanosecond level of precision.

A critical part of the timing circuit operates at the 10Hz cycle rate of the booster synchrotron. For this application, the timing circuit can synchronously detect a 10 Hz signal from the booster while it is running and use this signal to time the trigger for the 100MeV linear accelerator (LINAC) which directs electrons into the booster synchrotron. The detected 10Hz signal is derived from a so-called 'peaking strip' that senses when the booster has the correct magnetic field at the beginning of each 10Hz cycle to accept electrons from the LINAC.

It is desirable to keep the LINAC operational at all times, including between 5 minute SPEAR3 injection intervals in order to keep the temperature constant for optimum beam stability. In practice, however, the booster isn't always running for the sake of conserving power so the peaking strip does not deliver a 10Hz timing signal at all times. In this case, when the booster is in the 'power conservation' mode, the timing circuit uses a 10Hz clock signal derived from the 60Hz power line frequency supplied by Pacific Gas & Electric (PG&E) to trigger the LINAC.

The timing circuit developed for this purpose must continuously switch between the two 10Hz trigger input sources (PG&E and the booster peaking strip signal) in order to maintain a steady source of trigger pulses for the LINAC. Since the two 10Hz timing pulse sources are not precisely related with one another in time, glitches have been detected during the clock switching operation. This causes some injection cycles to be lost and thus is undesirable. In addition, the 10Hz timing signal from the peaking strip is known to 'slew' in time as the booster ramps up and down with potential detrimental results to high power electronic equipment. The purpose of my project was, therefore, to design and build a glitch-free 10Hz clock multiplexing circuit as an upgrade to the present timing system for the SSRL booster synchrotron.

II. Technical Approach and Methodology

After carefully studying the present timing circuit, we identified the necessary input/output signals required to construct a replacement timing circuit. As mentioned above, the inputs include the 10Hz timing clock derived from PG&E line power and the 10Hz peaking strip signal available at 5 minute intervals during booster operation. The output is either the 10Hz PG&E signal or 10Hz peaking strip signal depending on the 'SELECT' state internal to the circuit. Based on this information, we developed a rough schematic of an "upgraded" timing circuit which included a reportedly glitch-free clock multiplexing circuit. The schematic helped us to envision how the multiplexing circuit would operate technically and how it would be integrated into the present timing system.

a. The Glitch-Free Clock Multiplexing Circuit

The prototype switching circuit was selected based on an article published in the EE|Times journal[1]. The glitch-free digital clock multiplexer circuit is shown schematically in Fig. 2. To demonstrate how the circuit operates, examination of the circuit shows that if both input clocks (CLK0 and CLK1) are running, when the "SELECT" signal is in the "LOW" state, the output of the "AND1-1" gate is also "LOW" This means the data input of the D-type flip-flop DFF1-1 is also "LOW" and thus its "Q" output is "LOW". At the same time the "Q" output of DFF1-2 is also "LOW" since its data input is the "Q" output from DFF1-1. This configuration drives the output of the gate AND1-2 to "LOW". As a result, CLK1 cannot propagate to the output of the multiplexing circuit.

In this state both inputs to AND0-1 are "HIGH" since the "Q_N" output of DFF1-2 is the complement of its "Q" output and INV1 inverts the "LOW" state "SELECT" signal into "HIGH". Therefore, the data input of DFF0-1 is driven "HIGH". As a result, its "Q" output also goes "HIGH" which drives the data input of DFF0-2 "HIGH". This, in turn, drives the "Q" output of DFF0-2 to "HIGH" when CLK0 is "HIGH". This holds one input to AND0-1 at a steady "HIGH" state. Its output then follows the other input from CLK0. Therefore, whenever the "SELECT" signal is "LOW" CLK0 is propagated to the output of the circuit through gate OR1.

1. An online electronics industry magazine published in the United States by UBM, Canon

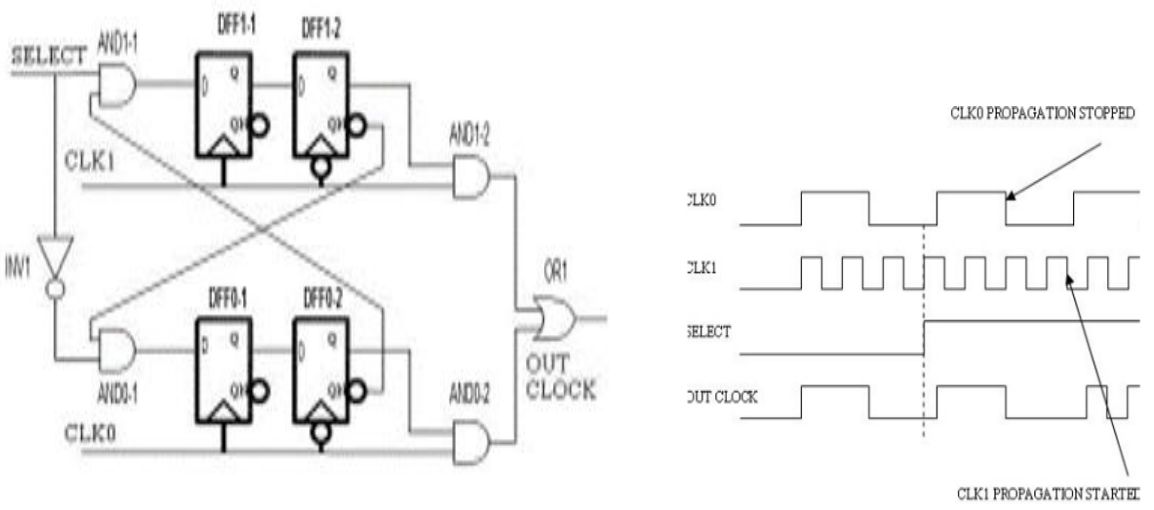


Figure 2: Glitch-free clock multiplexing circuit (left), input/output waveform (right)

Conversely, when the “SELECT” signal toggles to “HIGH”, INV1 changes one input to AND0-1 into a “LOW” state. The output of AND0-1 then changes to “LOW” which in turn drives data input to DFF0-1 to “LOW”. The “Q” output of DFF0-1 is then forced into “LOW” which in turn drives the “Q” output of DFF0-2 to “LOW”. This de-selects CLK0 by forcing the output of AND0-2 to “LOW”. At the same time, the complement output “Q_N” of DFF0-2 changes into “HIGH” which in turn drives the output of AND1-1 to “HIGH”. This forces the output of DFF1-1 into “HIGH” which also in turn drives the output of DFF1-2 into “HIGH”. The result is that one input to AND1-2 is held at a steady high state and thus its output follows its second input which is CLK1. This way, CLK1 is propagated through the output of the clock multiplexing circuit whenever the SELECT signal is high.

Significantly, the arrangement of the two negative-edge triggered D-type flip-flops (DFF1-2 and DFF0-2) assures that the selection control is registered at the falling edge of the clock signal and that the selection is enabled only after the existing clock is de-selected which remarkably avoids the problem of having glitches at the output of the clock multiplexing circuit (see EE|Times article, p. 2). Moreover, the use of a positive edge triggered D-type flip-flop in each of the two clock selection paths prevents a phenomenon called meta-stability related to asynchronous input signals (EE|Times article, p. 4).

For the application at the SSRL booster synchrotron, the 'SELECT' capability can be used for remote control of switching between the 10Hz PG&E and the peaking strip clock pulses. By interfacing with the main control system, a remote command can be issued to drive the SELECT line high or low depending on the state of the synchrotron i.e., when the booster synchrotron is fully 'ON' the SELECT line can be used for timing based on the peaking strip and when the booster synchrotron is 'OFF' the 10Hz clock derived from PG&E can be used as a 'housekeeping' signal.

b. Circuit Synthesis

For a preliminary test of the EE|Times circuit we first constructed a prototype configuration on a breadboard. The breadboard can supply integrated circuit bias voltages, a stable ground plane and easy access to test points. For this phase of the project no soldering was required. Figure 3 shows a design sketch of the timing circuit in which the clock multiplexer will be incorporated and Fig. 4 shows a photograph of the circuit layout on the breadboard.

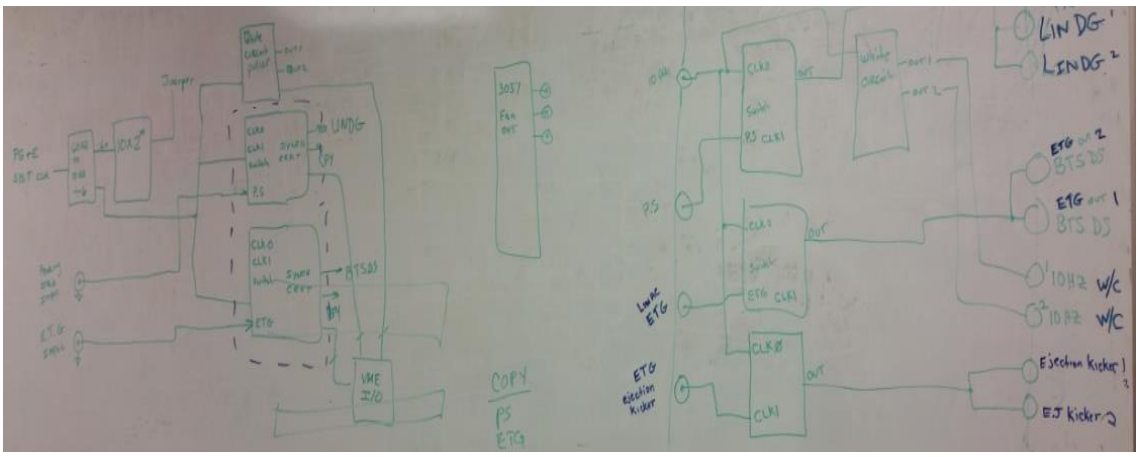


Figure 3: A preliminary sketch of the new timing circuit.

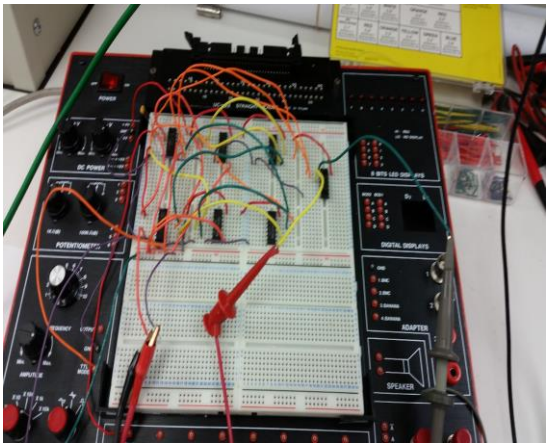


Figure 4: Breadboard circuit construction.

After careful assembly of the multiplexer circuit on the breadboard and review for any wiring or assembly errors, we proceeded to testing. We injected two different clock signals CLK0 and CLK1 into the circuit and examined the output on a TDS 3054B oscilloscope to see if the circuit responded correctly to the SELECT line and was glitch free. The clock signals came from an SRS DG535 and a Hewlett Packard 3245A digital delay generators. These delay generators were so useful in the test and evaluation process, because it was easily possible to examine the multiplexer over a wide range of clock frequency and pulse width. We used a 5 Volt DC (direct current) source connected to the "SELECT" terminal through a mechanical switch to simulate switching of the SELECT signal. The idea is that as we turn the mechanical switch "ON" or "OFF", the "SELECT" terminal of the switching circuit gets connected to or disconnected from a 5 volts DC source. This simulates a logic state of "HIGH" or "LOW" respectively which in turn makes the multiplexer output toggle between the two input clock signals (in practice the 10Hz PG&E and peaking strip clocks).

With breadboards, however, the connecting wires are simply plugged into pinholes and thus the connections are not as tight as soldered connections. This fact makes breadboards susceptible to noise, especially in applications involving high frequency signals. Our ultimate goal was to build this circuit and test it by connecting into the real booster synchrotron machine. With this

drawback, however, the breadboard would not be a good fit for the purpose. Therefore, after making sure that the circuit was glitch-free, we proceeded to building the circuit on a prototype 'vector board'. We decided to mount the vectorboard in a 19" chassis and use BNC connectors for input/output interface.
Vectorboards are more solid than breadboards. They also have better connection to the outside and have less noise than breadboards as connections are made by soldering terminals together. They also allow flexible construction of the circuit layout. Since the circuit was going to be physically plugged into the machine, we had to be extra careful in making sure that we considered all the factors necessary for the final test. A couple of circuit design meetings were undergone to take the project to the next level. As a result, few upgrades were made to the breadboard configuration which included adding a set of integrated-circuit driver chips to achieve impedance matching (see Appendix). The resulting circuit constructed on the vectorboard is shown on the left in Figure 5. Notice the universal connector pins on the edge of the board. These make it easy to plug in and unplug the board. The complete chassis is shown on the right in Figure 5. The chassis can contain up to three parallel multiplexer boards. For our purpose, we decided to build one complete channel first for the LINAC application and test it on the running machine during dedicated testing time. Then once we got the result that we expect, we can later construct multiple copies of the circuit and plug into the multi-pin connectors.

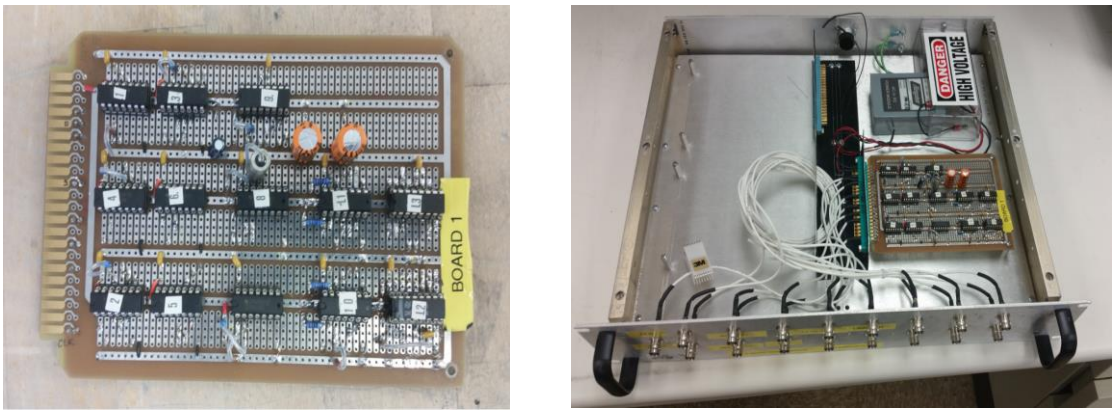


Figure 5: EE|Times multiplexer circuit constructed on a vector board and installed in a 19" chassis.

c. Diagnostic Testing

The testing and diagnostics process comprised of two phases. First, we conducted bench testing by injecting clock input signals from the delay generators and monitoring the output on the oscilloscope. We observed the behavior of the circuit using clock inputs of different frequencies and pulse width. Then as a final test to verify circuit functionality, the system was physically transported to the booster synchrotron and installed in parallel with the operational timing circuit using 8ns BNC cables. For the PG&E clock we inserted a 50 Ω in-line resistor at the output and routed the clock signal to both our prototype multiplexer box and the oscilloscope. The peaking strip clock was available from an auxiliary port on the peaking strip processor chassis. Both 10Hz input clocks and the multiprocessor output were visible on the oscilloscope.

We also connected the output from the in-situ multiplexer to the oscilloscope to view the live output trigger controlling the LINAC. Similarly, a parallel output channel from the in-situ module known as the 'Extraction Trigger ' (ET) was monitored to learn how the timing circuit operates at the top of the 10Hz booster acceleration cycle.

III. Result

The result of the diagnostic tests conducted in the lab as well as on site were as follows.

1. In-lab Test

While bench testing the clock multiplexer using diagnostic test equipment, we found that it was correctly switching between the two clock inputs (in both breadboard and vectorboard assemblies) without any glitches. However, we also learned that a single pulse was missing from the multiplexer output signal. This happened every time the multiplexer switched from one clock input to the other.

2. On-line Test

Figure 6 shows the oscilloscope traces based on the nominal, in-situ 10Hz multiplexing circuit. To the left is shown the oscilloscope trace of the situation when the booster is off (no peaking strip input). The scope was triggered by the PG&E clock seen as the white vertical bar under orange 'T' symbol. The LINAC trigger appears 40ms later in purple and the extraction trigger 75 ms later in green. Both the LINAC and ETG triggers have delay internal to the in-situ multiplexer box. The oscilloscope trace to the right shows the scenario when the peaking strip is active (negative-going blue trace). In this case, there is no 40 ms time delay between the peaking strip and LINAC trigger pulse, by design. Note that both the LINAC trigger and ET trigger signals jitter with respect to the PG&E timing reference. The primary reason for the multiplexer circuit is to compensate for the jitter by triggering directly from the peaking strip clock (either the existing circuit or our circuit).

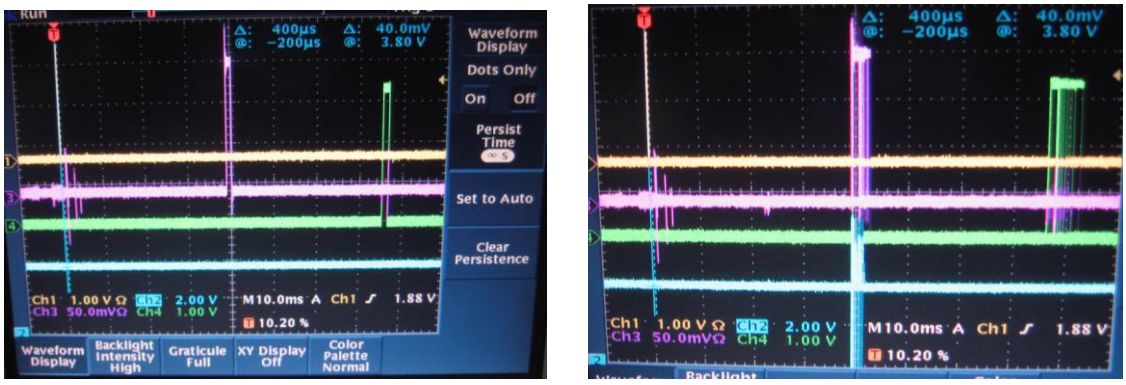


Figure 6: LINAC and ETG triggering with in-situ multiplexer. (left) booster off, (right) booster on.

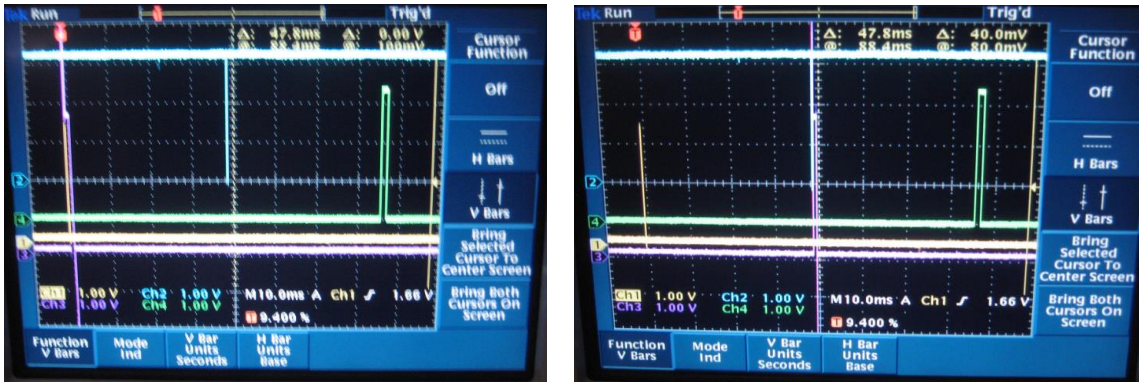


Figure 7: LINAC and ETG triggering with EE|Times multiplexer. (left) booster off, (right) booster on.

Figure 7 shows the same timing information using the EE|Times multiplexer chassis. In this case, again triggering on the PG&E clock, we see to the left that the LINAC trigger appears promptly after the PG&E trigger when the booster is off. A 40ms delay was expected but is not present. To the right is shown oscilloscope trace when the booster is 'ON'. The EE|Times multiplexer has been switched to trigger on the peaking strip clock input. Here the LINAC trigger appears promptly after the peaking strip as it does with the in-situ timing circuit (see Figure 6, on the right).

VI. Summary and Conclusion

We constructed a digital electronic multiplexing circuit to switch between 10Hz trigger sources derived from PG&E and the SSRL booster synchrotron peaking strip, respectively. The circuit configuration was based on a "glitch-free" switching topology published in EE|Times. First tests were carried out on an electronic breadboard taking advantage of the bias voltage capability, ground plane and easy access to test points. Independent signal generators were used to provide clock inputs CLK0 and CLK1. Both different frequencies and similar frequencies were used from two separate waveform generators. Once the breadboard tests were complete, the circuit was reconstructed on a compact 'vectorboard' with universal mounting pins. In this case dip sockets were used for the integrated circuit chips with jumper wires soldered directly to the board. This provided a more stable configuration relative to the push-pin breadboard tests. The vector board was then installed in a 19" rack-mountable chassis populated with multiple BNC input/output ports for easy input/output access and diagnostic capability. Digital clock generators were again used in conjunction with an oscilloscope to verify performance of the switching circuit.

As a final test, it was possible to parasitically tap in to the main booster synchrotron timing circuit while the accelerator systems were fully operational. For these tests a copy of the 10Hz 'heartbeat' timing clock derived from PG&E was connected to CLK0 and the 10Hz peaking strip clock connected to CLK1. When the booster was operational, we demonstrated that cycling the SELECT switch HI/LOW correctly resulted in either the PG&E signal or peaking strip signal transmitted to the multiplexer output. In the process of these tests we detected several shortcomings of the EE|Times multiplexer circuit design as applied to our booster synchrotron switching situation. In the first case, it was recognized that the EE|Times circuit cannot 'switch' unless both clocks are present. For our application when the booster turns off, the peaking strip clock is disabled. So the multiplexer circuit cannot switch back to PG&E as by design it requires the two clock inputs to be present in order to switch from one to the other. In addition, we found that the present in-situ multiplexer applies a 40ms

delay to the PG&E input prior to triggering the LINAC systems. Even though this feature can easily be added with fine adjustment on the delay, our clock multiplexer does not have it at the present time. The response of both multiplexers to the peaking strip input is prompt in both cases. In conclusion, we determined that this clock multiplexing circuit-even if it cleanly switches between the two clock signals without glitches-is not yet ready to be incorporated in the present timing circuit. Before it can be deployed to upgrade the present timing system, certain feature need to be added among which the ability to self-switch (giving priority to the peaking strip clock whenever it is available and only switching to the PG&E clock when the peaking strip clock is missing) and putting a 40 ms delay on the output trigger signal when the clock from PG&E is selected are the most important.

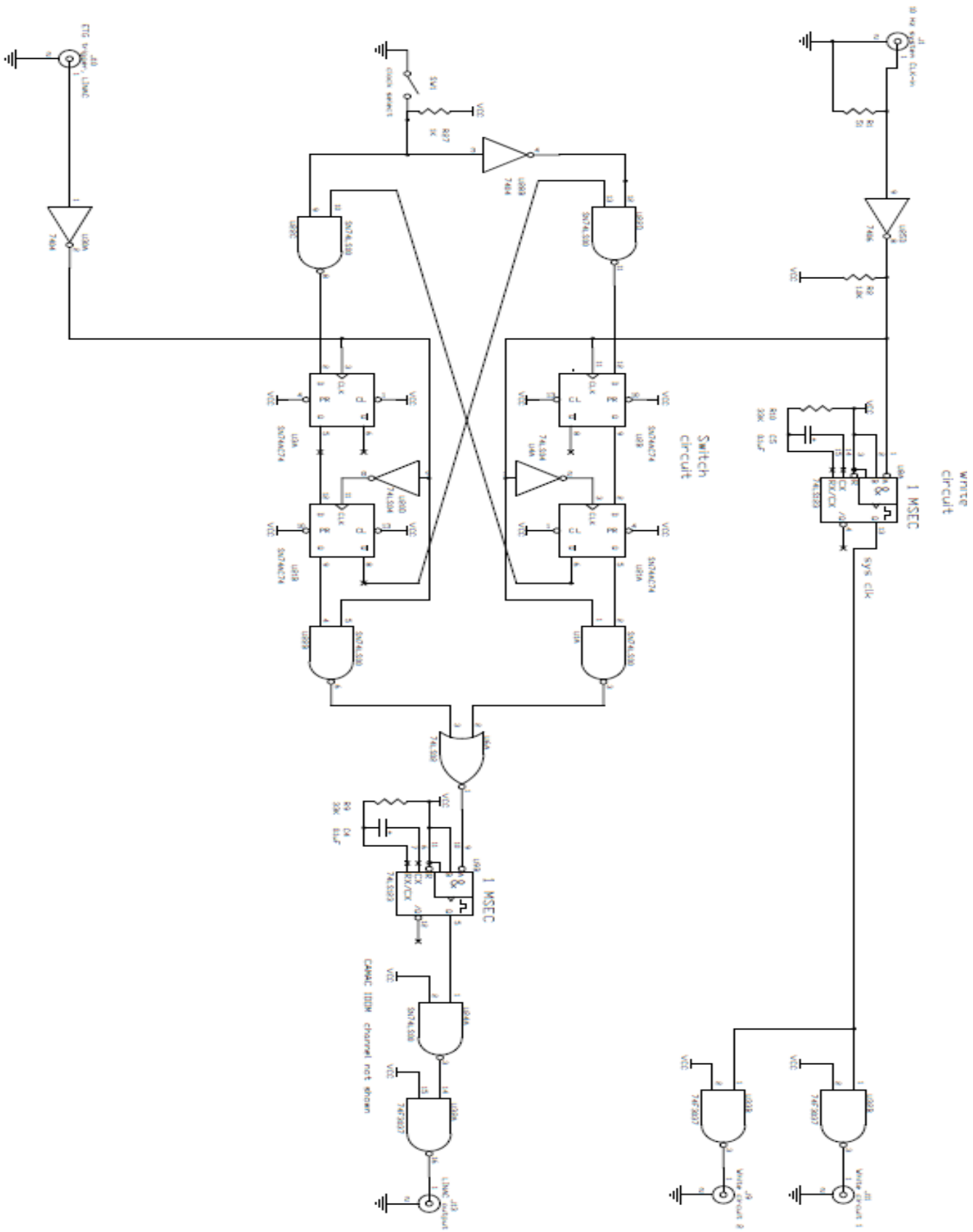
ACKNOWLEDGEMENTS

Special thanks to Jeff Corbett and Don Martin for being wonderful mentors for this project. Rich Burgess taught me many basic principles of digital electronics and helped me each step of the way during this project. Thanks also to SPEAR3 technicians Scott Wallters and Steve Berry for their invaluable help throughout this project. Finally, thanks to SLAC and the DOE for providing this research opportunity through the CCI program.

REFERENCES

Mahmud, Rafey. “Techniques to make clock switching glitch free”. EE Times. np. June 30, 2003. Web. June 22, 2015.

Appendix


Switch circuit
write circuit
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