SLAC-WP-121

Building a Better Capacitor

Enjoy the journey

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Office of Science, Science Undergraduate Laboratory Internship (SULI) Program

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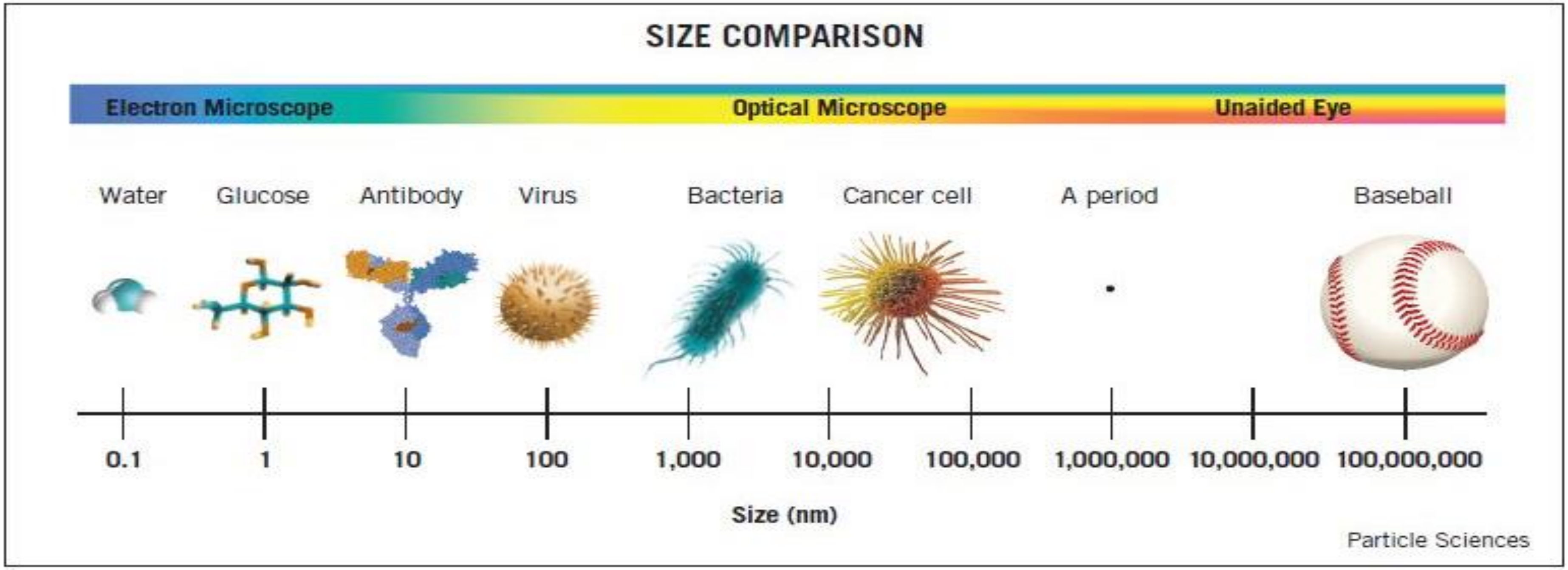
Abstract

The goal of this research is to determine procedures for creating ultra-high capacity supercapacitors by using nanofabrication techniques and high k-value dielectrics. One way to potentially solve the problem of climate change is to switch the source of energy to a source that doesn't release many tons of greenhouse gases, gases which cause global warming, into the Earth's atmosphere. These trap in more heat from the Sun's solar energy and cause global temperatures to rise. Atomic layer deposition will be used to create a uniform thin-film of dielectric to greatly enhance the abilities of our capacitors and will build them on the nanoscale.

Overview

- Basic concepts.
- Why do you care?
- Photolithography, a basic overview
- Pictures and samples
- Acknowledgements
- Q&A
- Win a prize? It could be you!

What is Nano?

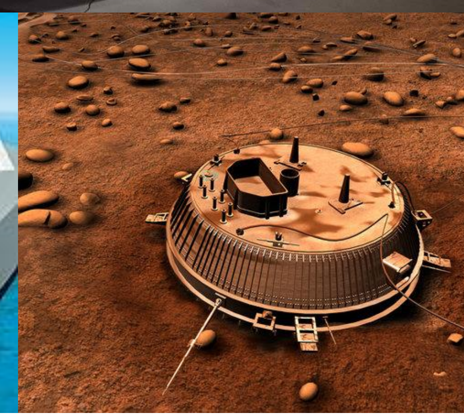


- Sheet of paper: 100,000 nm
- Human DNA: 2.5 nm diameter
- Single Au atom: 0.3 nm
- Fingernails grow 1 nm a second

http://www.particlesciences.com/services/micro-nano-technology/

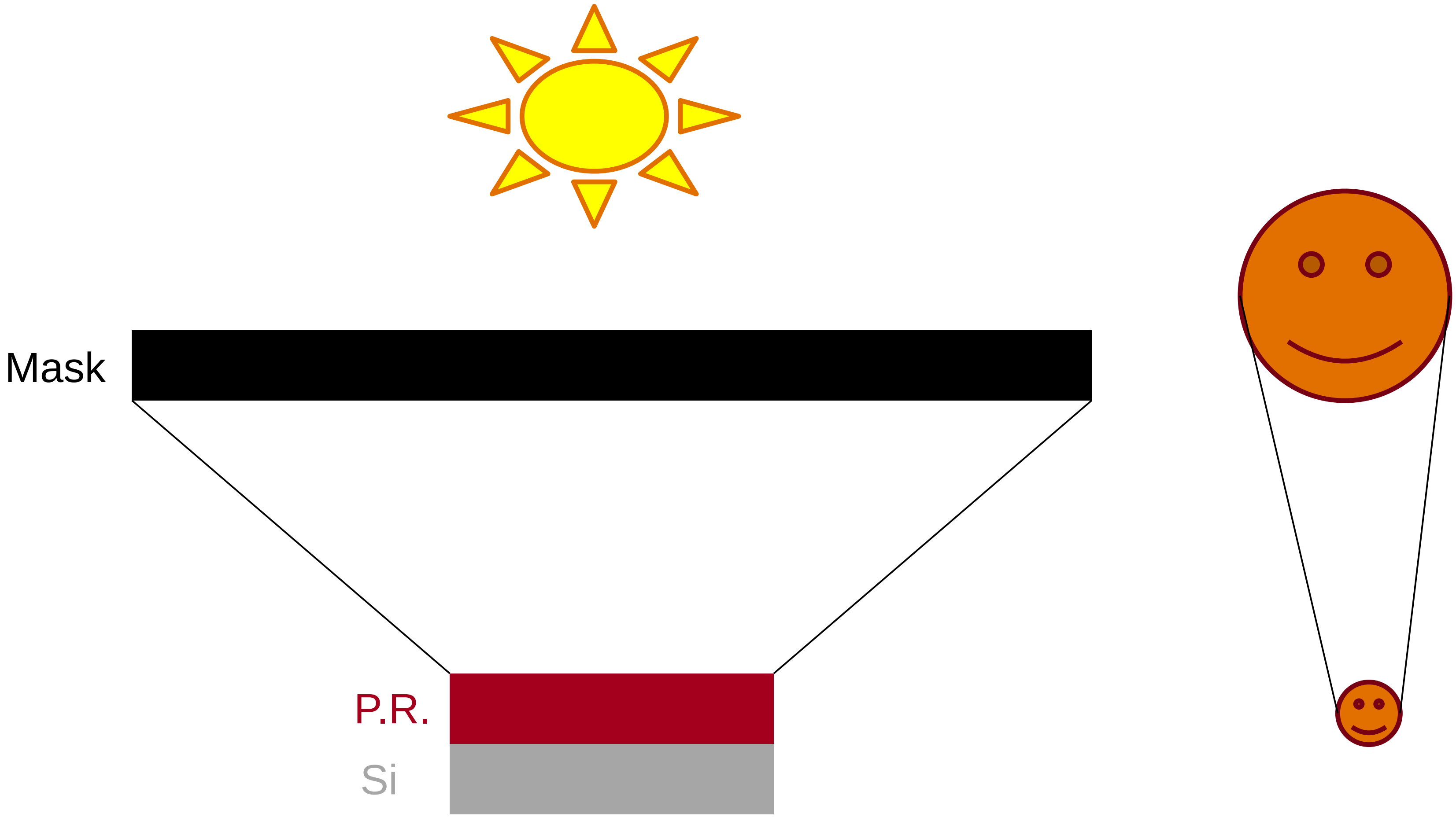
Why Super Capacitors?

- Quick charge/discharge rate.
- Better acceleration for electric cars.
- No chemical reactions.
- Can operate in extreme environments.
- Smaller consumer devices.
- Ideal for The Internet of Things
- $C = \frac{k\varepsilon A}{d}$



- http://www.esa.int/Our_Activities/Operations/Cassini-Huygens
- http://www.wired.com/2007/01/us_navy_invents/
- https://www.flickr.com/photos/cytech/7163567282/

Photolithography



Photoresist (PR)

- PR is dripped onto wafer.
- Wafer is spun at high speeds to create a uniform thickness.
- Baked shortly to prepare PR for exposure.

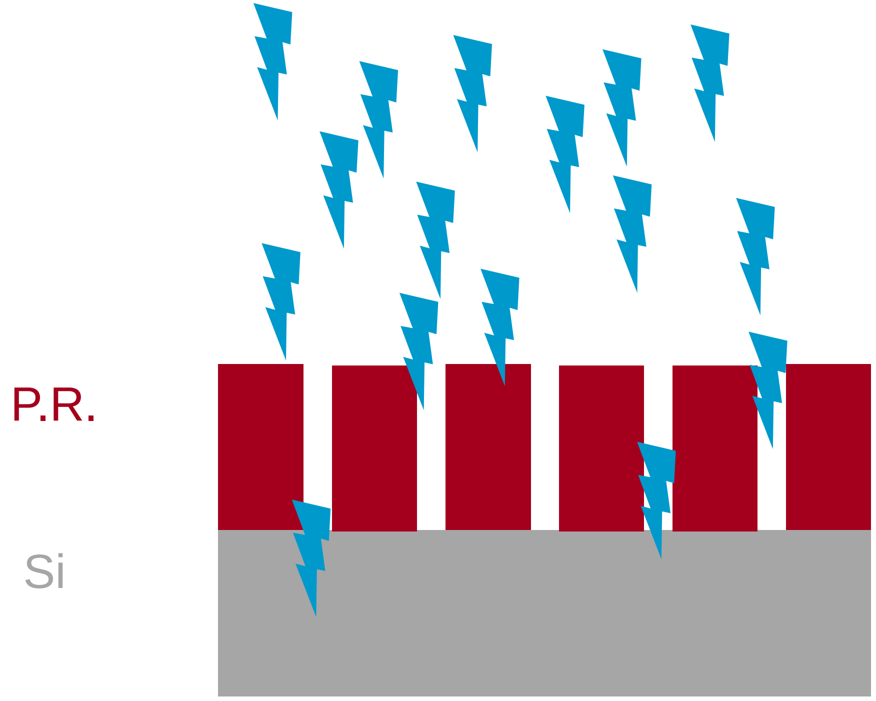
Picture source: https://commons.wikimedia.org/wiki/File:Photoresist_spin_coating.jpg

Photolithography (Develop step)

- Cross-links within the PR get broken → exposed areas become more soluble.
- Chemical developer removes PR.

Etching

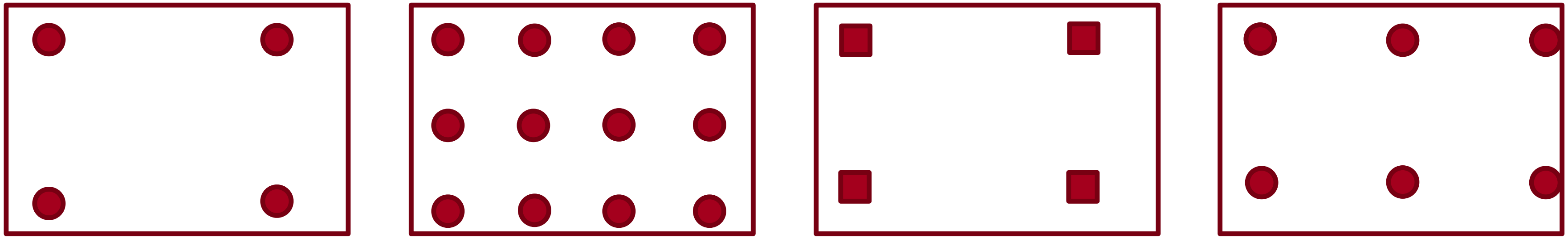
- Dry etching process: Reactive Ion Etching.
- Bombard wafer with plasma SF_6
- P.R. protects covered area.



Final Result

My Design

- 4 different 3D capacitors to be tested.
- All had a feature size of .5 µm
- Cap 1 & 3: pitch of 4 µm
- Cap 2: pitch of 1 µm
- Cap 3: pitch of 2 µm



Cap 1 Cap 2 Cap 3 Cap 4

Not to scale.

Holes in Si (top view)

Cap 1 Magnification: 200 X

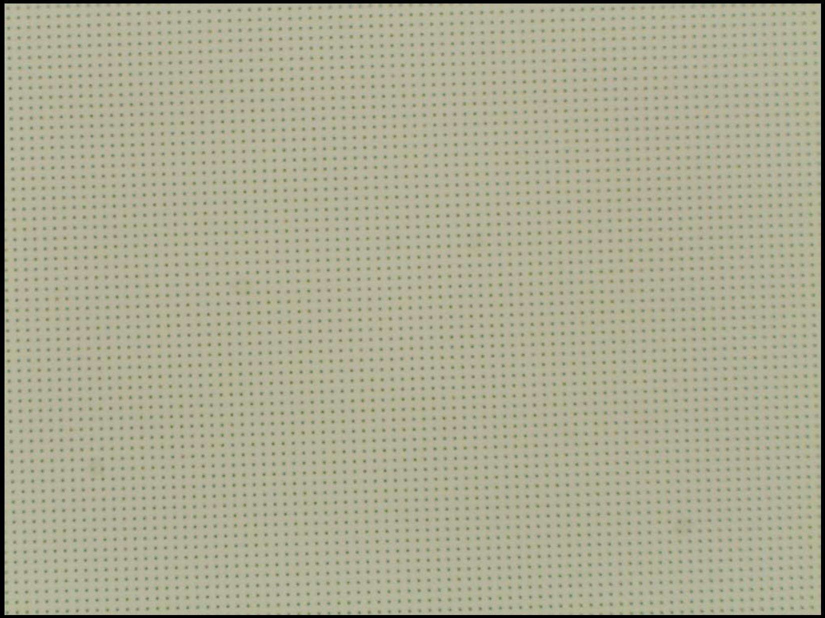
- Nearly Invisible
- Rarely present
- Almost missed it

Cap 2 Magnification: 200 X

- Horizontal gradients
- Inconsistent hole size

Holes in Si (top view, continued)

Cap 3 Magnification: 200 X



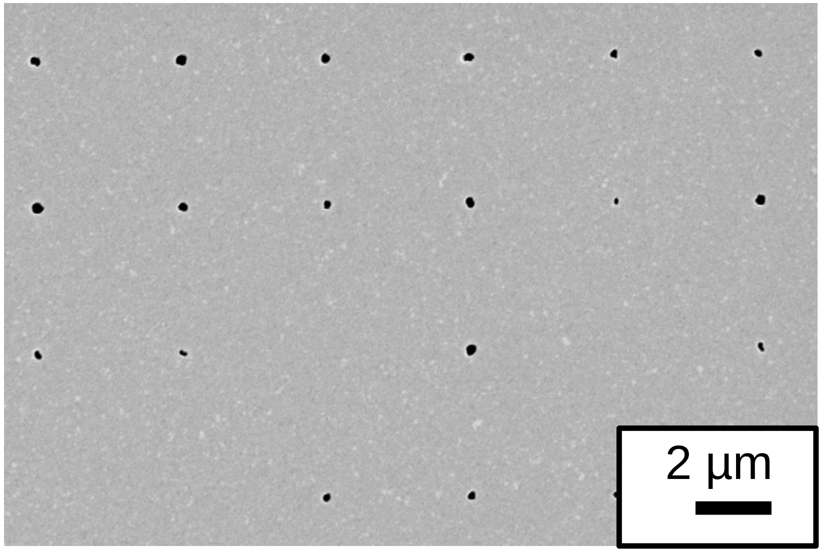
- Nearly perfect
- Diameters around 800 nm

Cap 4 Magnification: 200 X

- Spotty and inconsistent
- Better than Cap 1

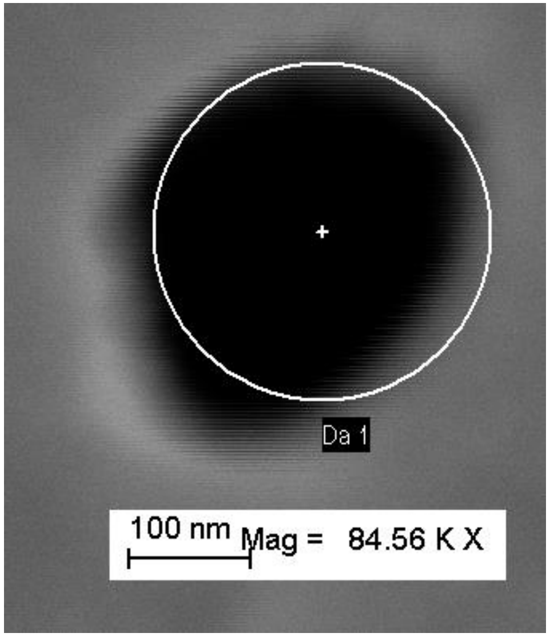
SEM Cap 1

Broad overview



- Typical
- Not good results
- 5,000 X

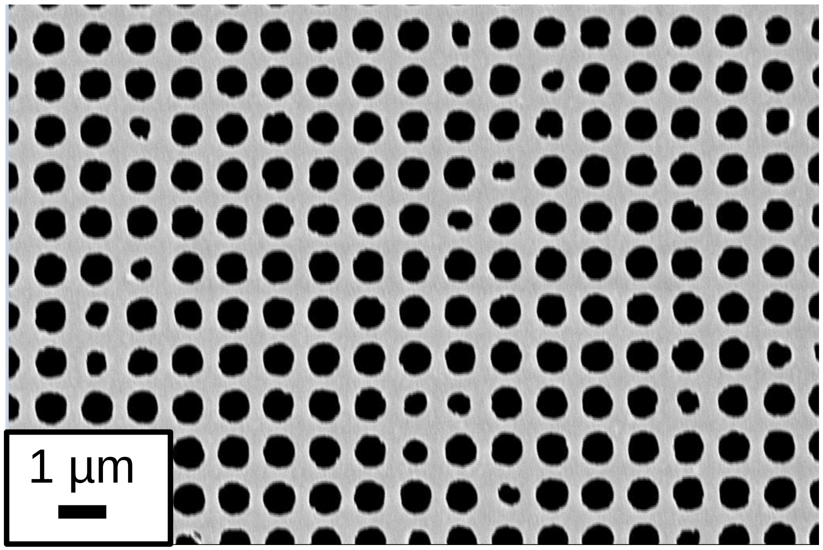
High magnification



- Diameter = 280 nm
- Small than visible light

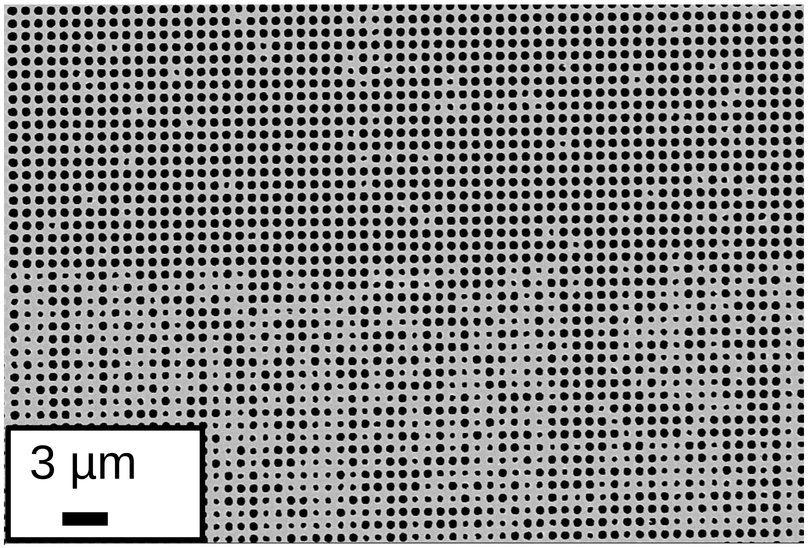
SEM Cap 2

Good placing



- Fairly consistent zoomed in.
- 6,000 X

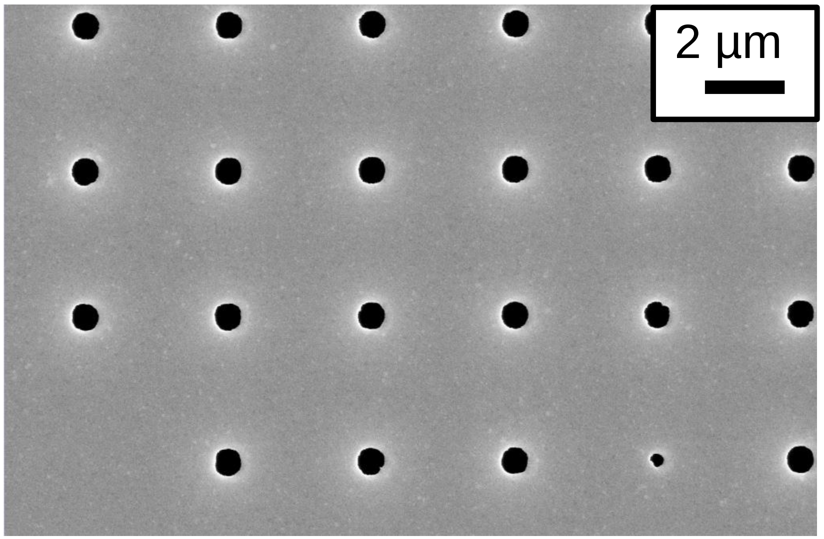
Gradient Zones



- Smaller holes on bottom.
- 2,000 X

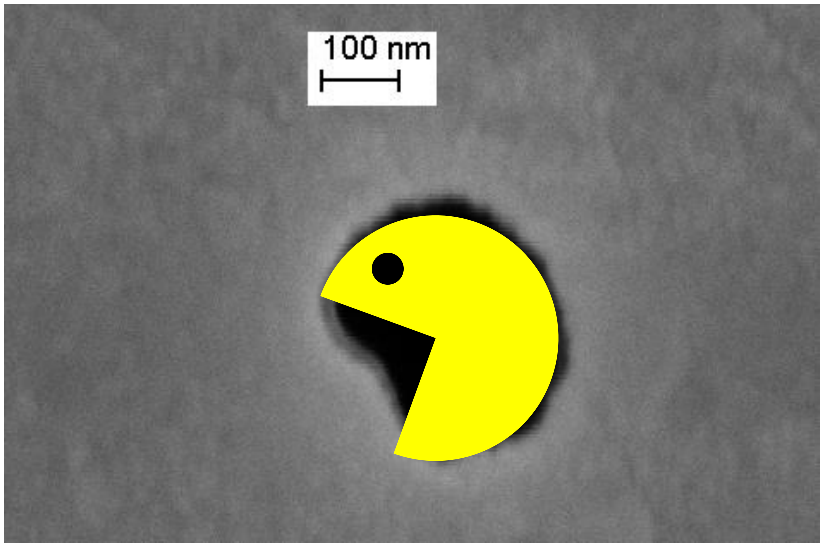
SEM Cap 3

Perfect Cap



- Worst area… still very good.
- 5,000 X

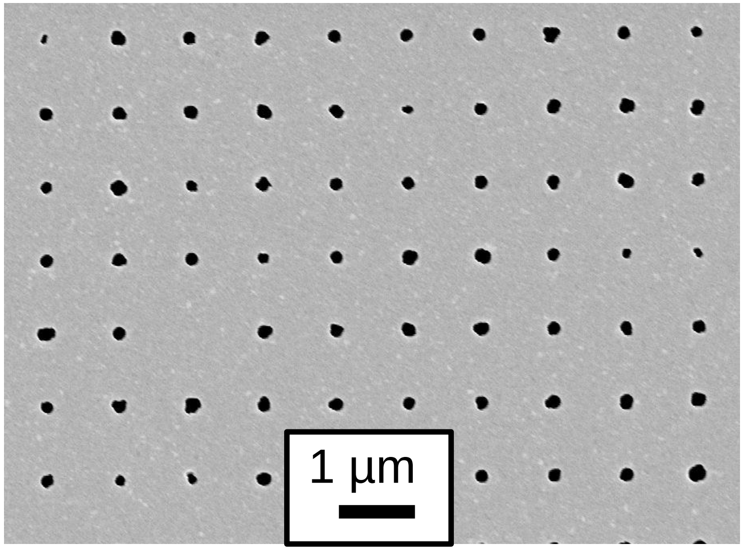
Single Hole



- Close up of non-uniform hole.
- 50,000 X

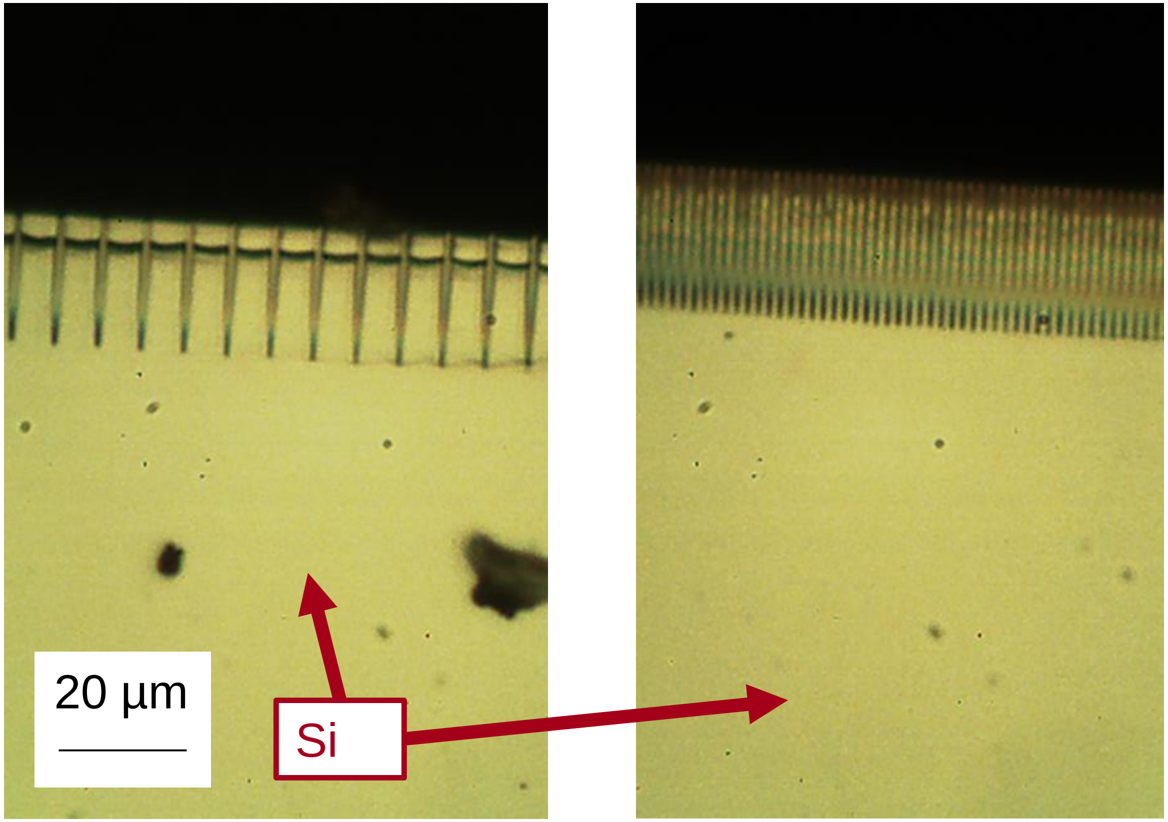
SEM Cap 4

Mediocre



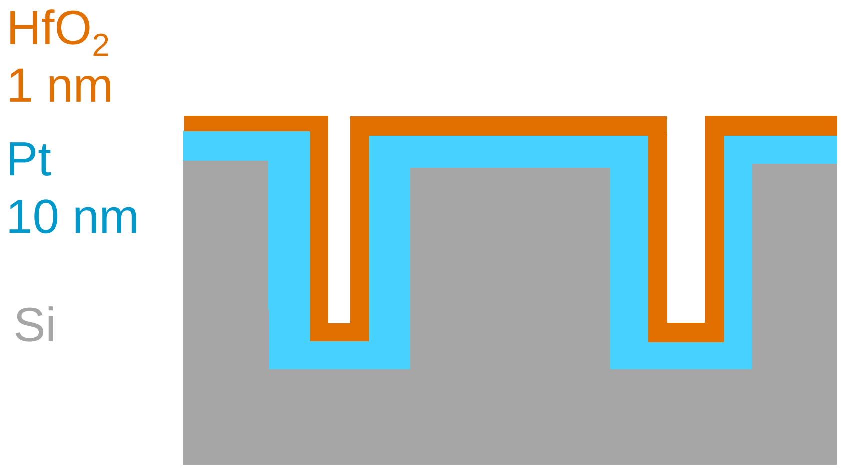
- 5,000 X
- Slightly better than Cap 1
- Only deserving of one picture

Holes in Si (side view)

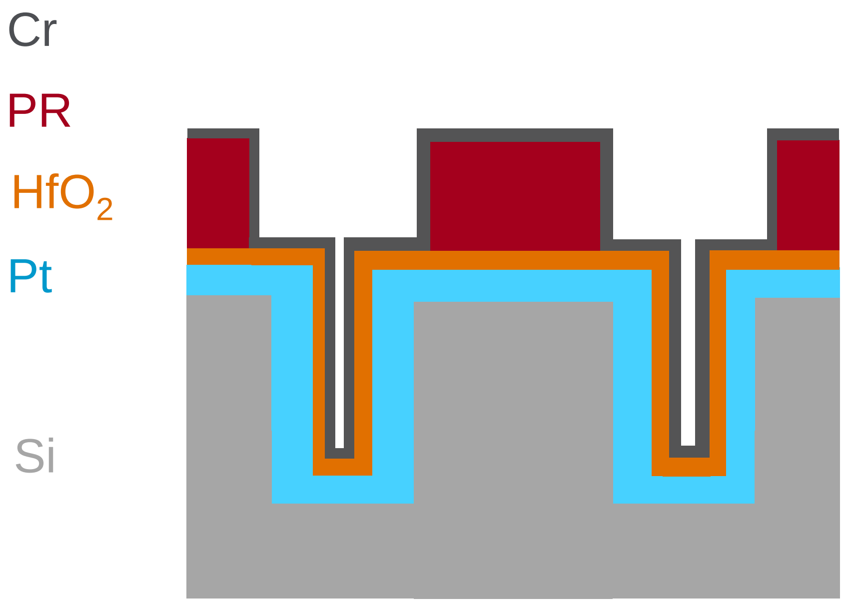


- Two different areas
- Cleaved wafer.
- 20 minutes of etching resulted in 20 µm depth.
- 30-40 aspect ratio

Atomic Layer Deposition



Liftoff



Liftoff

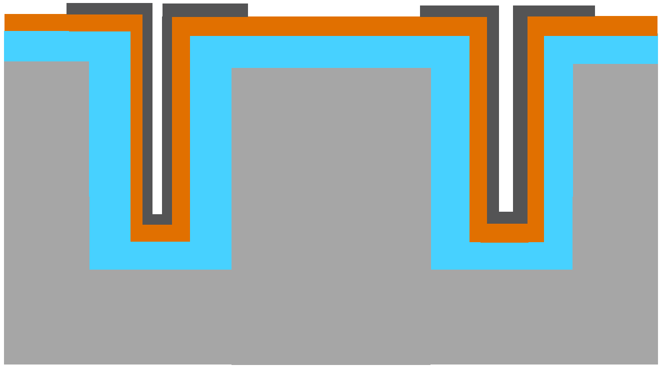
Cr

PR

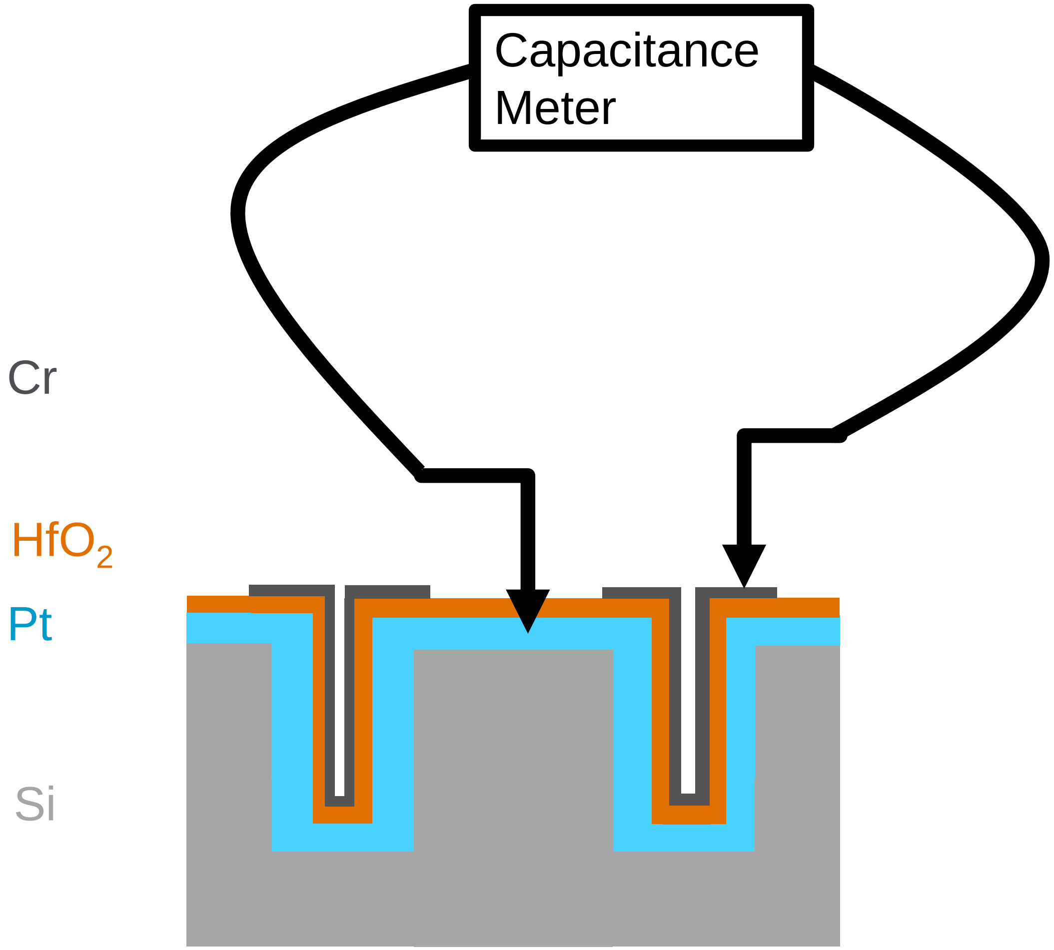
HfO_2

Pt

Si



Testing Capacitance



Conclusion and future work

- Get a reading!
- Test different insulating materials and thicknesses.
- Determine breakdown voltage and current leakage.
- Establish a consistent recipe.
- Squares are good.

Acknowledgments

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- Congratulations to all the SULI, CCI, and STAR summer interns, you survived!