EMCOR Test Document

Test Plan

Revision:	0.6
Status:	Draft
Repository:	Test Repository
Project:	EMCOR Controller
Folder:	SlacSpace -> Instrumentation and Controls Division -> Special Projects -> AIP: MCOR Controller
Document ID:	
File:	EMCOR-TestPlan.docx
Owner:	
Last modification:	August 19, 2015
Created:	October 9, 2014

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Document History

Revision	Date	Changed/reviewed	Section(s)	Modification
0.1	2014-11-17	Gasper Jansa		Initial version
0.2	2014-12-16	Tomo Cesnik	3, 4, 6	Added HW tests provided by Jeff, added CPU procedures provided by Thuy
0.3	2015-02-03	Tomo Cesnik	5, Appendix A	Added appendix A
0.4	2015-02-16	Tomo Cesnik	5	Added test tracking to chapter 5
0.5	2015-05-04	Briant Lam	All	Incorporated edits to clarify test procedure
0.6	2015-08-19	Briant Lam	3.3	Changed resistance thresholds

Scope

This document specifies the tests and procedures that are to be performed on each EMCOR controller board.

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No table of figures entries found.

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References

1. Introduction

1.1. **Overview**

Each EMCOR controller board should be tested before it is put into production. This document first defines the appropriate test environment and connections that need to be made for successful testing. Second all the tests are described, including functional, non-functional, configuration, manual and inspection ones. If the board passes all hereby defined tests, it is ready to be tested with EPICS specific tests.

2. Test Environment

2.1. Hardware

All tests in this document are performed on the SLAC premises with the test setup described in the table below.

Table 2-1: List of hardware in the test environment

ID	Hardware item
	EMCOR controller board
	EMCOR tester board
	P2 Marx Hardware Manager
	EMCOR Kontron CPU (COMe-cDC2 N270) with 2GB, PC2-6400, 800MHz, SoDimm RAM and heat sink installed.

2.2. Software

Table 2-2: List of software in the test environment

Software component	Version	Where installed
Linux RT		EMCOR controller board
Remote PCI access server		EMCOR controller board

3. Hardware tests

3.1. Visual inspection [TC-EMCOR-HW-01]

This test ensures that the new board is visually inspected for any obvious problems.

Pre-requisites

1. N/A

Test procedure

1. Check hardware board visually with magnifying glass. Review/check/search for the following:

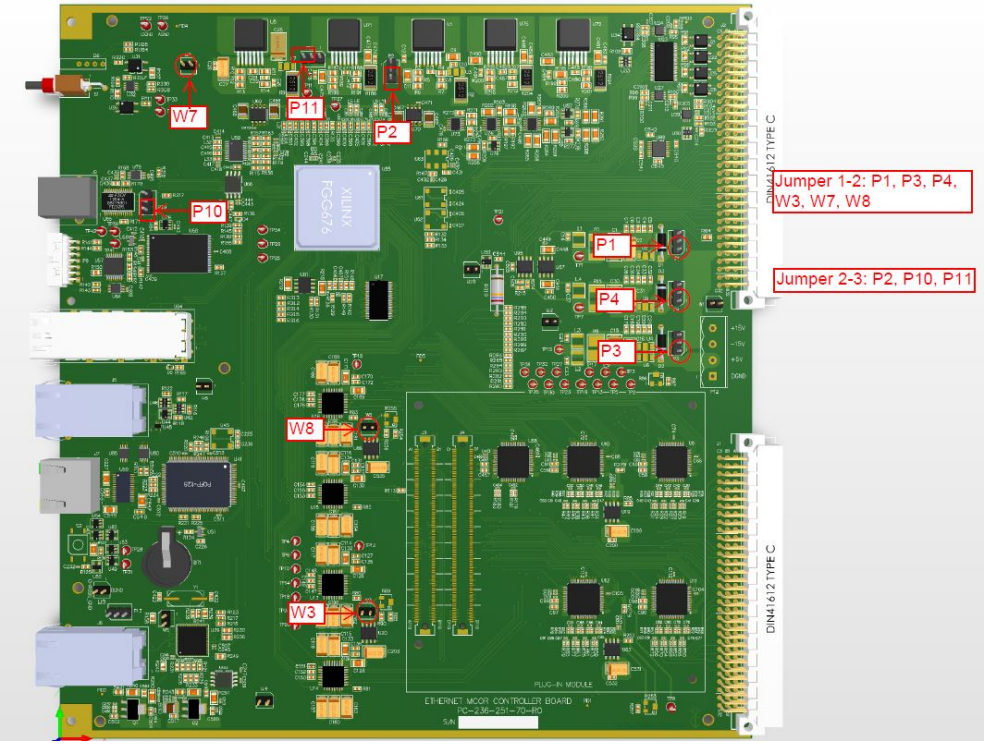
- PCB - search for any visual damage, board curvature, solder mask placement and quality, existence and quality of white text prints ...
- placement of integrated circuits, resistors, capacitors, optical module, connectors ...
- components mechanical or thermal damage
- quality of solder joins
- search for following soldering failures: solder shorts, solder wicking, solder drainage, tombstoning, drawbridging

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

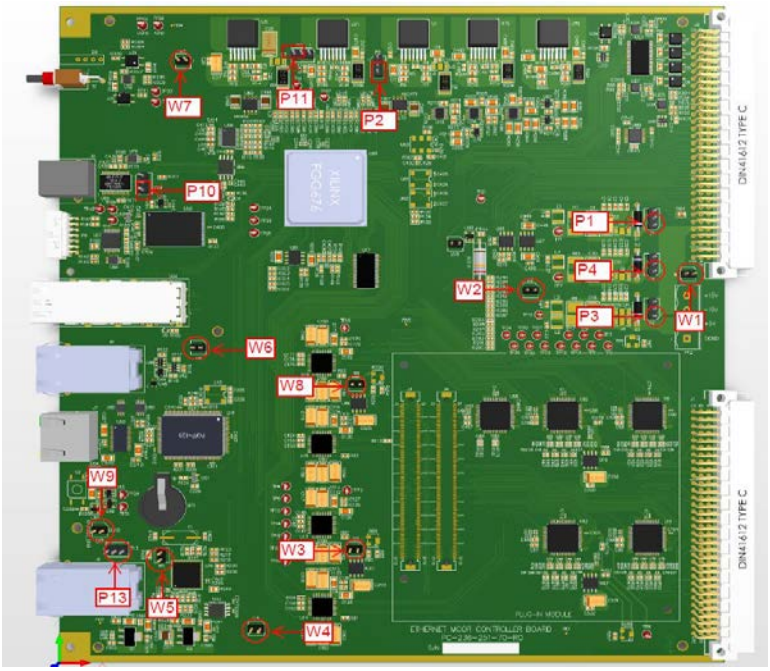
3.2. Install jumpers [TC-EMCOR-HW-02]

There are nine headers and jumpers on the EMCOR controller that need to be installed before you can start testing.



Header	Connection	1 - Signal	2- Signal	3- Signal	Use
P1	1 -> 2	+15_VIN_CRATE	+15V_IN	~~+15V_IN_AUX~~	+15V Power
P2	2 -> 3	~~+15V_IN~~	+3.3V	+5V_IN	+3.3V Power
P3	1 -> 2	+5V_IN_CRATE	+5_VIN	~~+5V_IN_AUX~~	+5V Power
P4	1 -> 2	-15V_IN_CRATE	-15V_IN	~~-15V_IN_AUX~~	-15V Power
P10	2 -> 3	~~3V3OUT~~	VCCIO	+3.3VCCIO	USB Output VCC
P11	2 -> 3	~~+15V_IN~~	+3.3VCCIO	+5V_IN	+3.3VCCIO Power
P13	?	DGND	MXCT	+1.9V	Ethernet IO Center Tap

Jumper	In/Out	1 - Signal	2 - Signal	Use
W1	?	DGND	AGND	Analog to Digital Ground Tie
W2	?	DGND	AGND	Analog to Digital Ground Tie
W3	In	+5V_REF1	+5V_REF1	DAC Reference
W4	?	DGND	AGND	Analog to Digital Ground Tie
W5	Out	ATEST_P	ATEST_N	Ethernet Controller DeBug
W6	?	DGND	AGND	Analog to Digital Ground Tie
W7	In	DGND	AGND	Analog to Digital Ground Tie
W8	In	+5V_REF2	+5V_REF2	DAC Reference
W9	Out	DGND	Chassis GND	Ethernet Connector Chassis Ground to Digital GND



3.3. **Power supplies resistance check [TC-EMCOR-HW-03]**

Manual check all power supplies resistance.

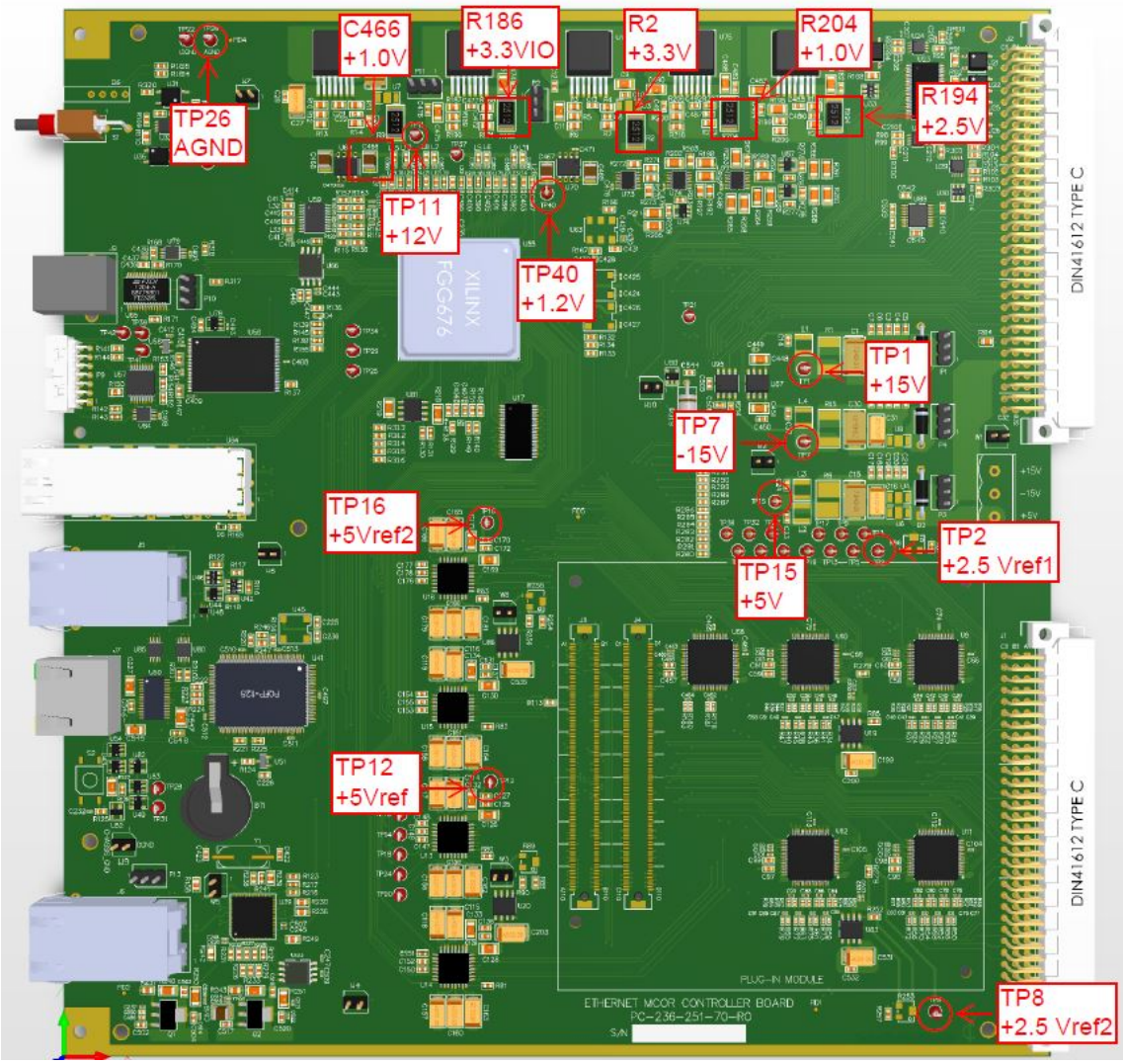
Pre-requisites

1. Procedure 3.1

Test procedure

With the CPU installed, (not shown in the diagram below) using a DVM, measure the resistance to ground on each of the power supplies.

1. Check DVM Battery level
2. Check DVM Lead Resistance. Record here: ☐
3. If the board does not pass the resistance check, do not plug the board into power.



Voltage	Location	Resistance	Limit	OK
+2.5Vref2	TP8		>5K	
+2.5Vref1	TP2		>5K	
+5V	TP15		>2K	
-15V	TP7		>4K	
+15V	TP1		>100K	
+2.5V	R194		>500	
+1.0V	R204		>30	
+3.3V	R2		>500	
+1.2V	TP40		>1K	
+3.3VIO	R186		>2K	
+12V	TP11		>2K	
+1.0V	C466		>2K	
+5Vref2	TP16		>10K	
+5Vref1	TP12		>10K	

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

3.4. **Voltages check [TC-EMCOR-HW-04]**

Manual check all voltages.

Pre-requisites

1. Procedure 3.3

Test procedure

Plug the P2 Marx Hardware Manager into the EMCOR tester. Then plug EMCOR tester into the EMCOR controller and turn on the power. Measure the voltages according to the table below.

Voltage	Location	Low Limit	Voltage	Upper Limit	OK
+2.5Vref2	TP8	2.485		2.513	
+2.5Vref1	TP2	2.485		2.513	
+5V	TP15	4.75		5.25	
-15V	TP7	-15.75		-14.25	
+15V	TP1	14.25		15.75	
+2.5V	R194	2.375		2.625	
+1.0V	R204	0.95		1.05	
+3.3V	R2	2.835		3.465	
+1.2V	TP40	1.14		1.26	
+3.3VIO	R186	2.835		3.465	
+12V	TP11	11.4		12.6	
+1.0V	C466	0.95		1.05	
+5Vref2	TP16	4.909		5.030	
+5Vref1	TP12	4.909		5.030	

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

3.5. **Calibration [TC-EMCOR-HW-05]**

Calibration of DAC/ADC.

Pre-requisites

1. Procedure 3.4

Test procedure

1. Adjust the following potentiometers such that the corresponding test points measure within ±0.001V of the specified value. Measurements are referenced to AGND, TP26:

Location	Voltage
R86, TP2	+2.500V
R253, TP8	+2.500V
R89, TP12	+5.000V
R255, TP16	+5.000V

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

3.6. **Program FPGA [TC-EMCOR-HW-06]**

Program the FPGA.

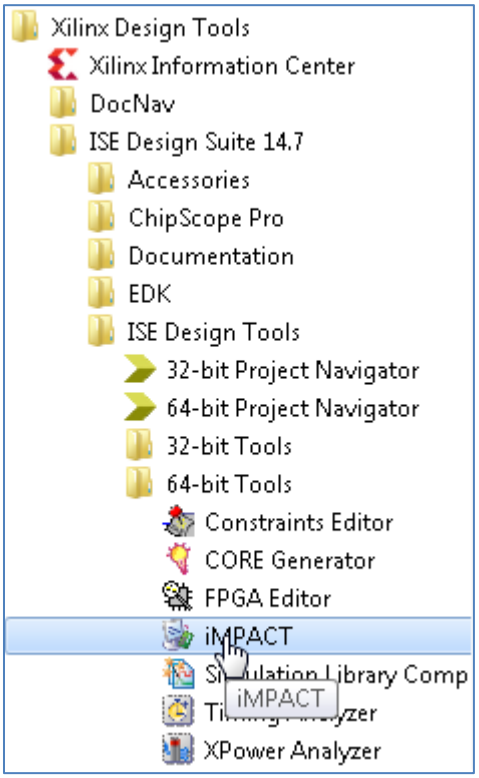
Pre-requisites

1. Procedure 3.5
2. A current copy of Xilinx iMPACT
3. Location of the Xilinx design file (xx.mcs)
4. Xilinx USB Programmer Platform Cable USB II

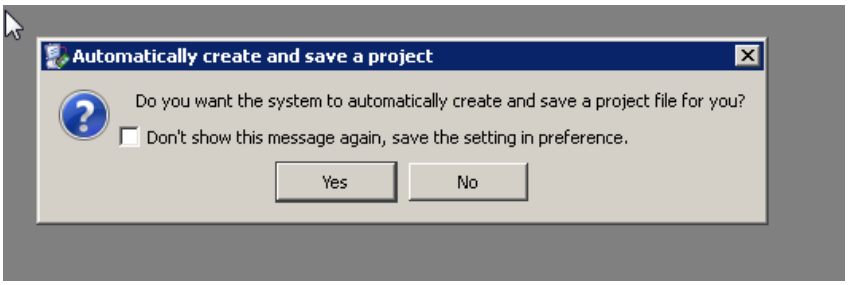
Test procedure

1. Connect the Xilinx USB programmer to the computer and the EMCOR controller board front panel (P9- JTAG PROG).
2. Power up the EMCOR controller.
   2.1. The green LED on the Programmer should light up at this time.
3. Start IMPACT on the computer either by clicking on the desktop icon

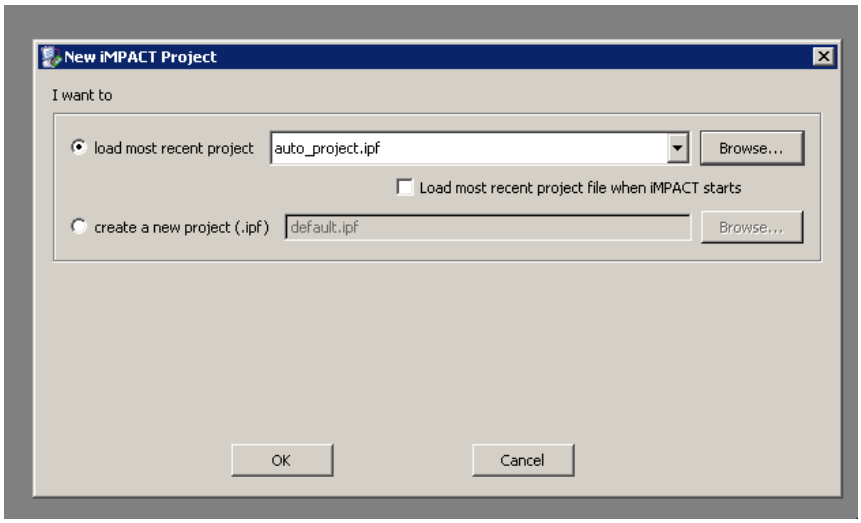
Or navigating from the Start Menu



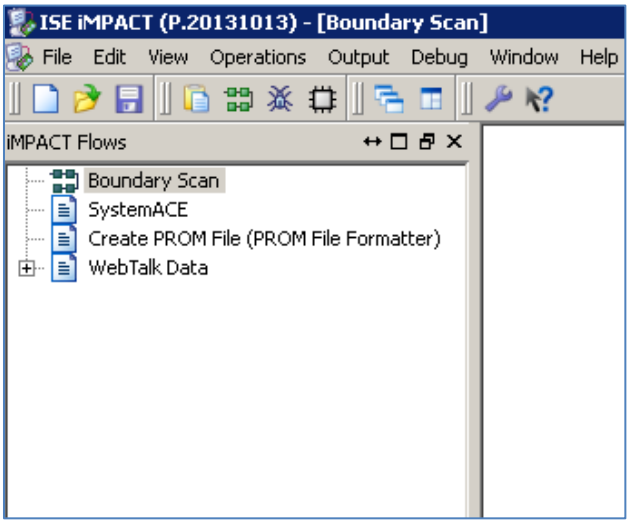
4. iMPACT will start with the »Automatically CREATE AND SAVE A PROJECT« pop-up dialog box. Click on »NO«.



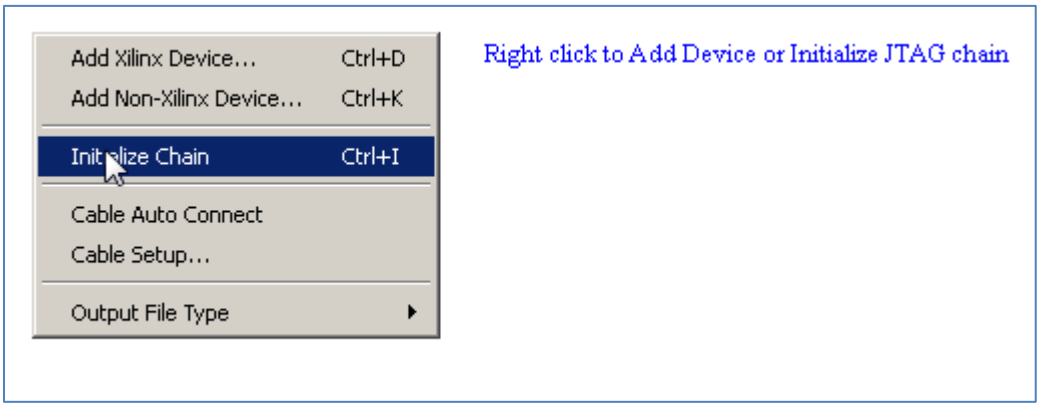
5. On the »New iMPACT Project« pop-up menu, select »Cancel«.



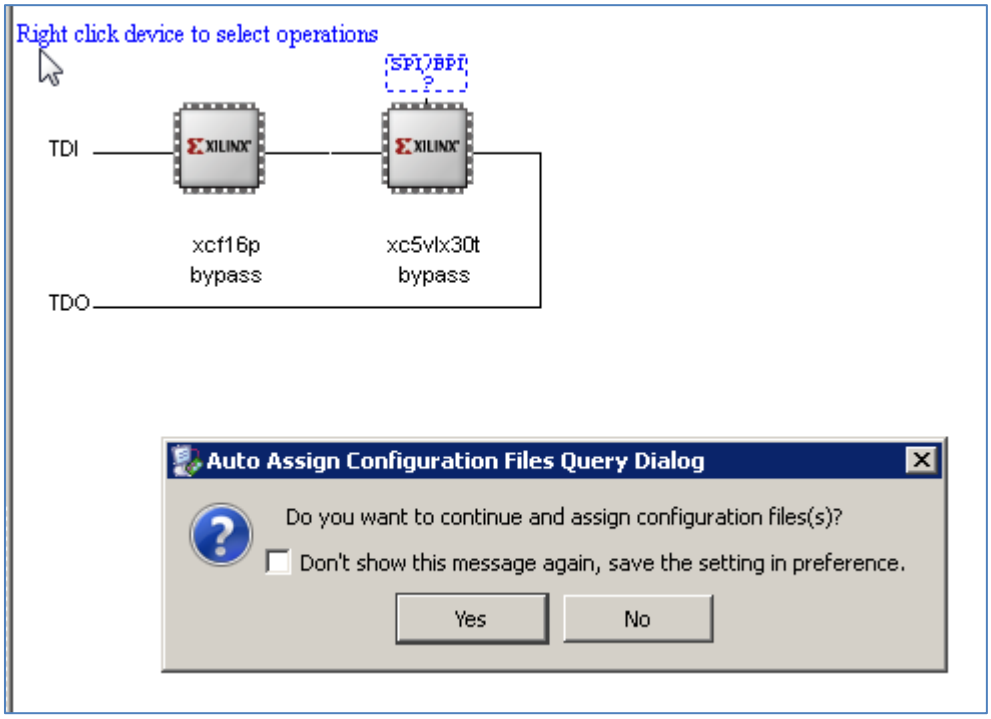
6. Double-Left-Click on »Boundary Scan« option in the window on the left.



7. The main screen will turn white and the text will say »Right click to Add Device or Initialize the JTAG Chain«. Right Click in the center of the screen and select »Initialize Chain«.

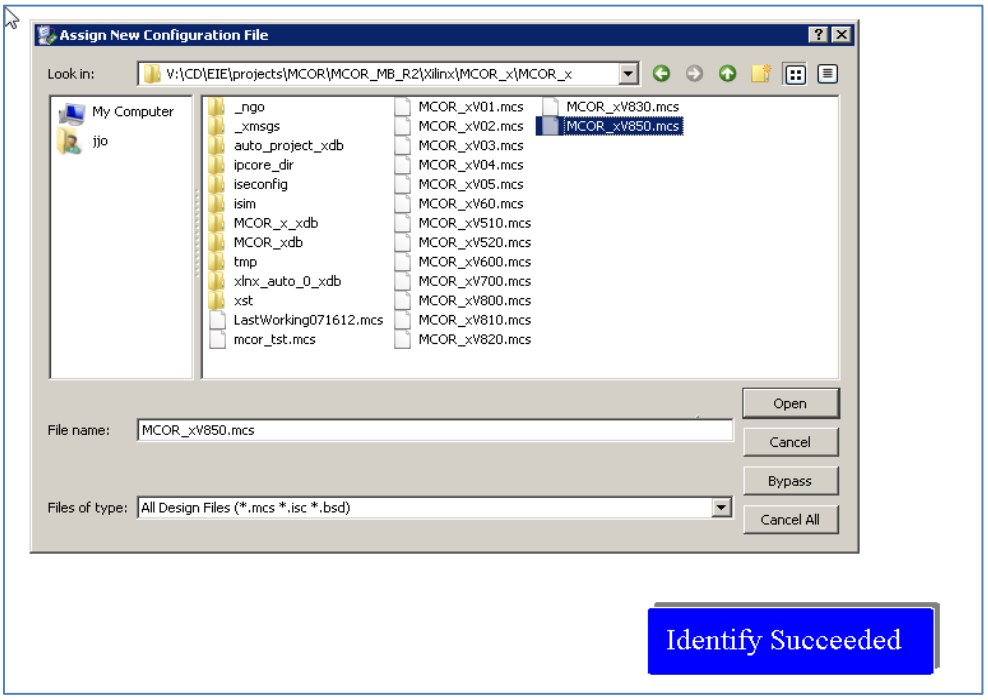


8. If the JTAG interface is connected correctly and working, the »Identify Succeeded« screen will appear.



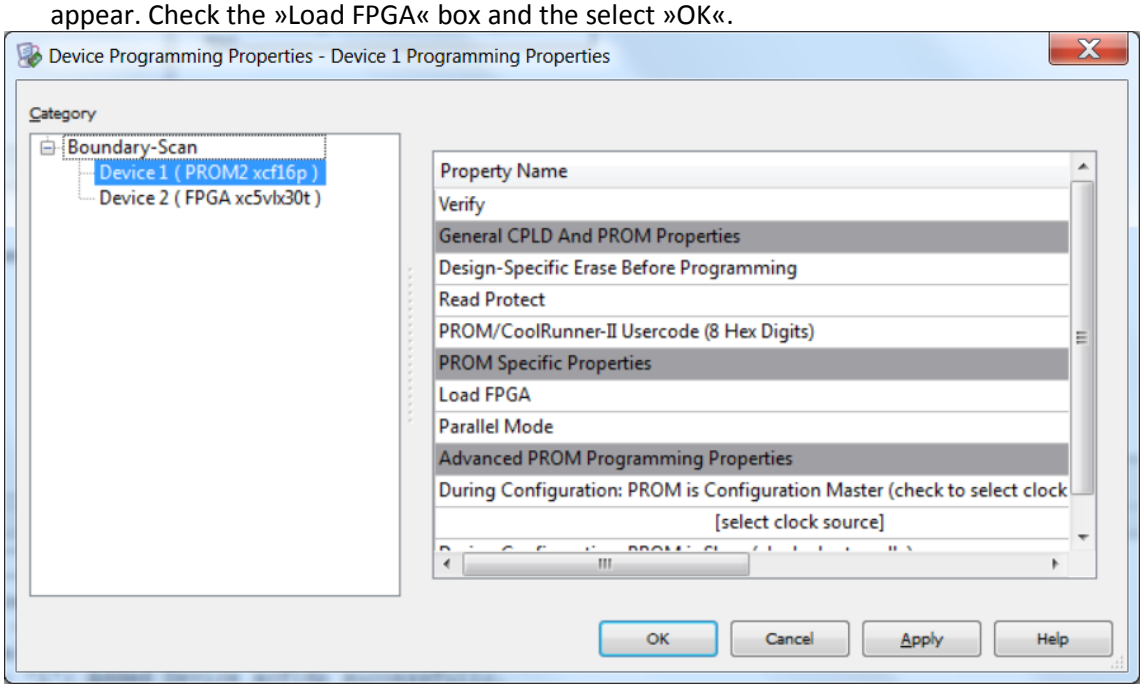
9. In the »Auto Assign Configuration Files Query Dialog« box, select »Yes«. The first device in the chain, xcf16p will be highlighted.

10. A file selection dialog box will appear. Navigate to the desired .mcs file. As of this writing, the file is at:
V:\CD\EIE\projects\MCOR\Ethernet_MCOR_Controller\Xilinx2Bar\MCOR_x\MCOR_x MCOR_xV901.mcs.
Click Open.

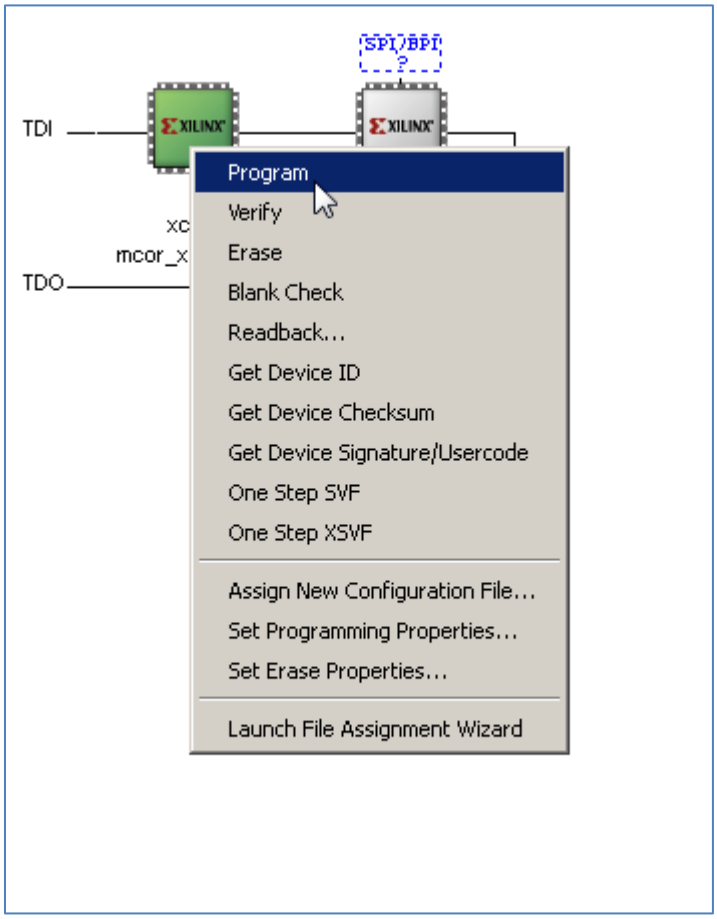


11. The second device in the string, xc5vlx30t will highlight and another file selection box will appear. Select »Bypass«.

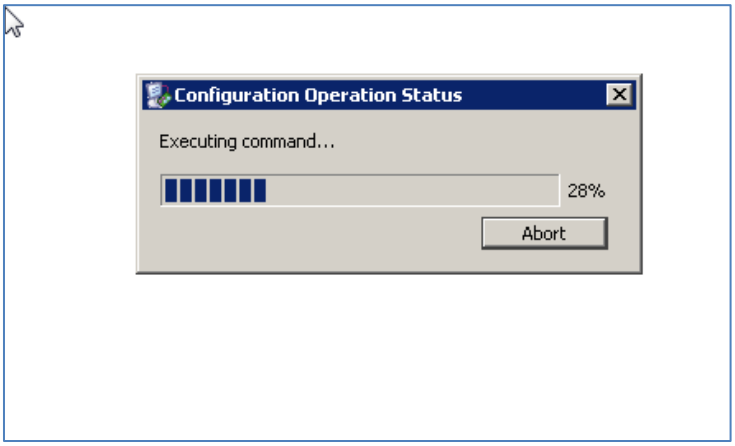
12. The »Device Programming Properties – Device 1 Programming Properties« dialog will appear. Check the »Load FPGA« box and the select »OK«.



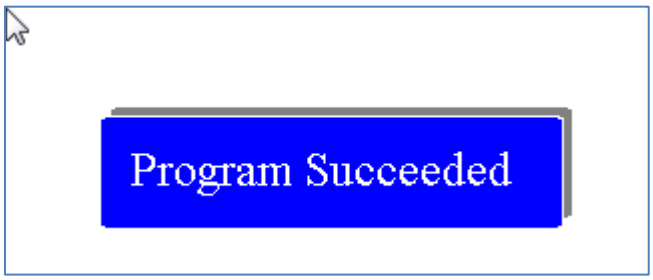
13. Right Click on the first device, xcf16p. It will highlight and a pop-up menu will appear. Select »Program«.



14. The »Configuration Operation Status« Menu will pop up.



15. The »Program Succeeded« window should pop up and the Xilinx is programed.



16. Power cycle the EMCOR controller. D4 on the EMCOR Controller should blink green and the »Fault« LED on the front of the EMCOR module should blink red.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

4. CPU/OS Tests

4.1. BIOS Setup [TC-EMCOR-CP-01]

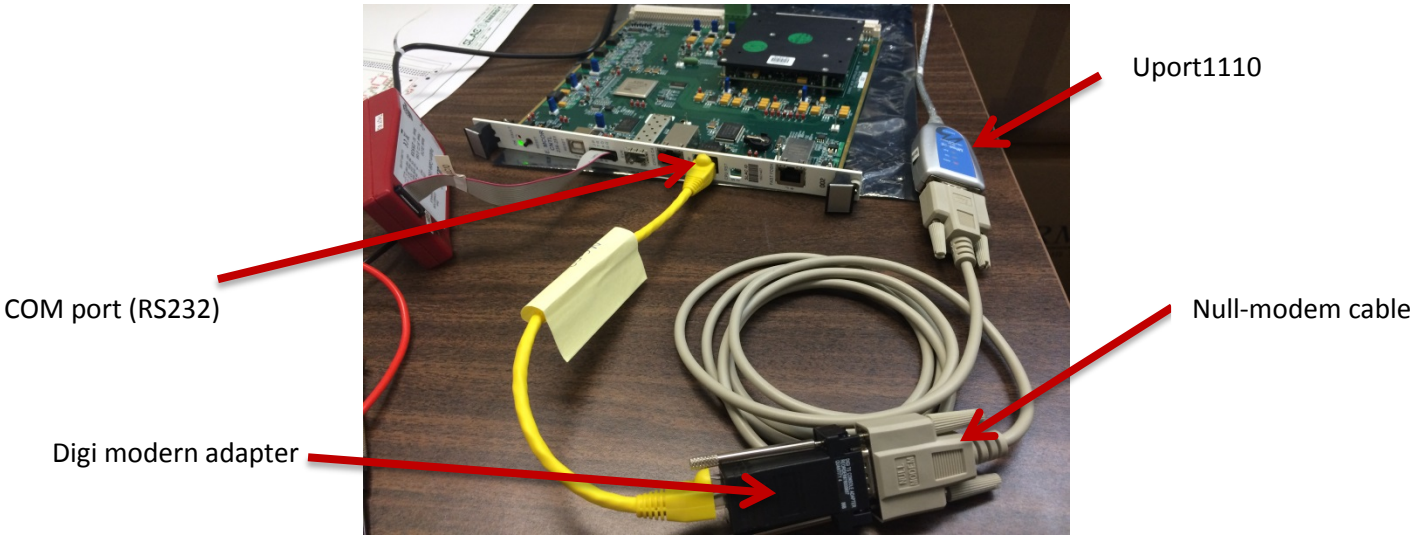
Setup the BIOS.

Pre-requisites

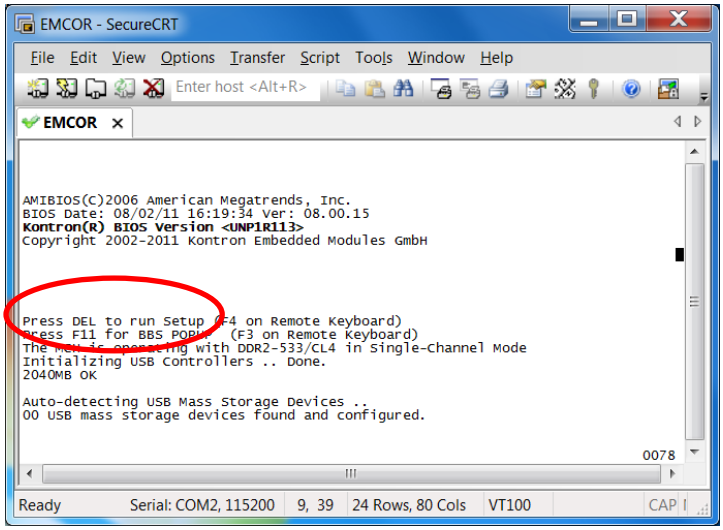
1. All hardware procedures

Test procedure

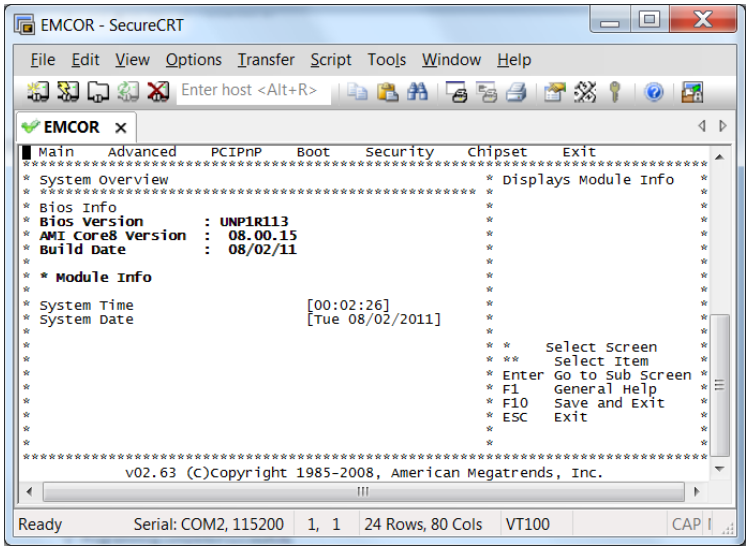
1. Request two node names to get IP addresses: one for Channel Access and one for Fast Feedback. Request NFS access for Channel Access so screen log file can be saved in $IOC_DATA location.
2. Connect COM port (RS232) using Digi Modern Adapter, null-modem cable, USB to serial converter Uport1110. Connect to laptop and start secureCRT 7 program. Set serial terminal configuration (under session options) as 8N1, Baud rate 115200, no flow control.



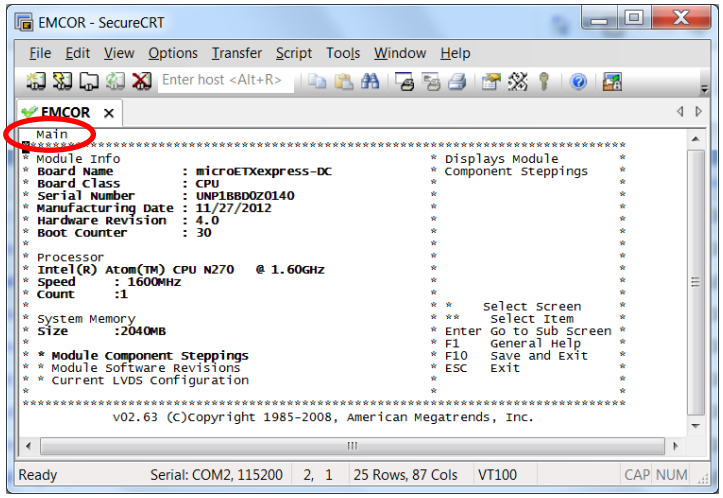
3. Connect PS (-15V to 15V) to P12 to turn on the EMCOR controller. When see the prompt on screen below, hit <del> key to enter BIOS set up.

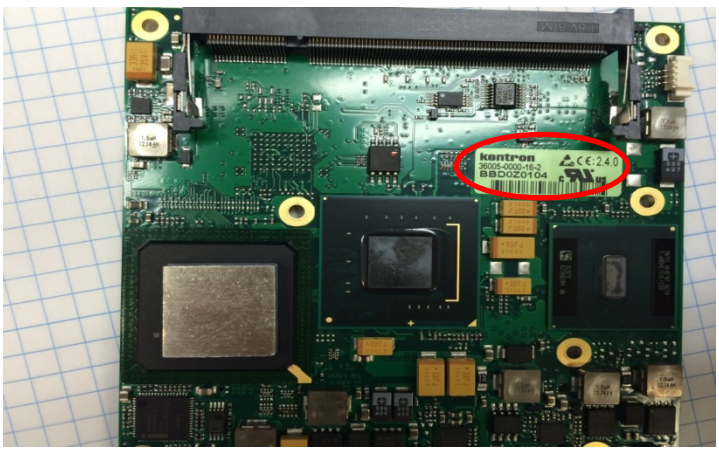


4. From >>System Overview<< we can see Bios Version.

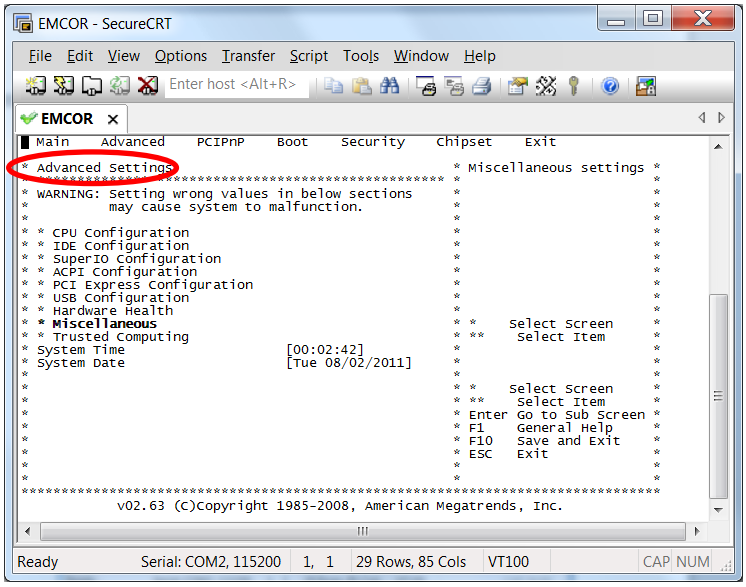


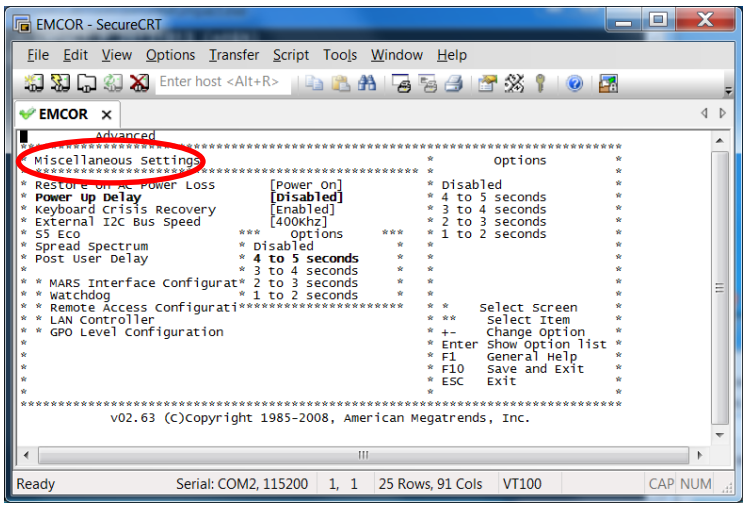
5. Use arrow key to move to »MAIN« Menu. Obtain serial number and processor information for Depot purposes or to contact vendor on future issues. (The serial number and part number can be seen when the heatsink and RAM are removed.)



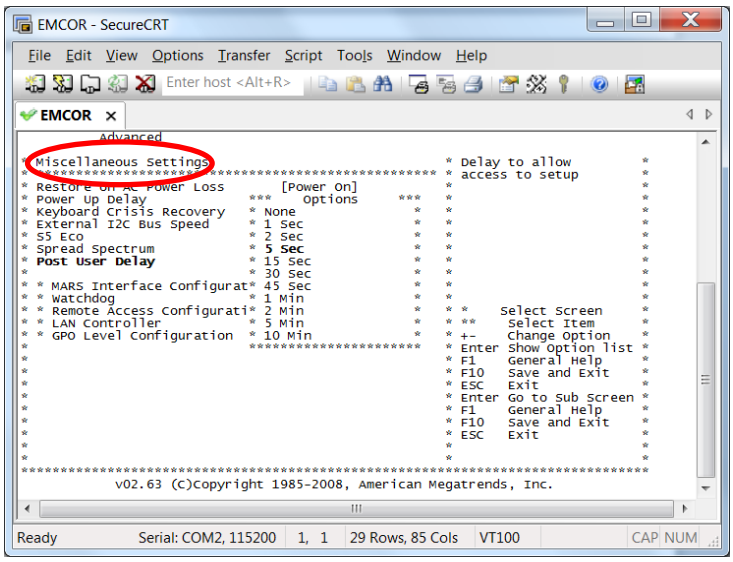


6. Use arrow key to move to »ADVANCED« Menu. Then, go to »Miscellaneous«, select »Power Up Delay«, scroll down to »4 to 5 seconds« and hit Enter.

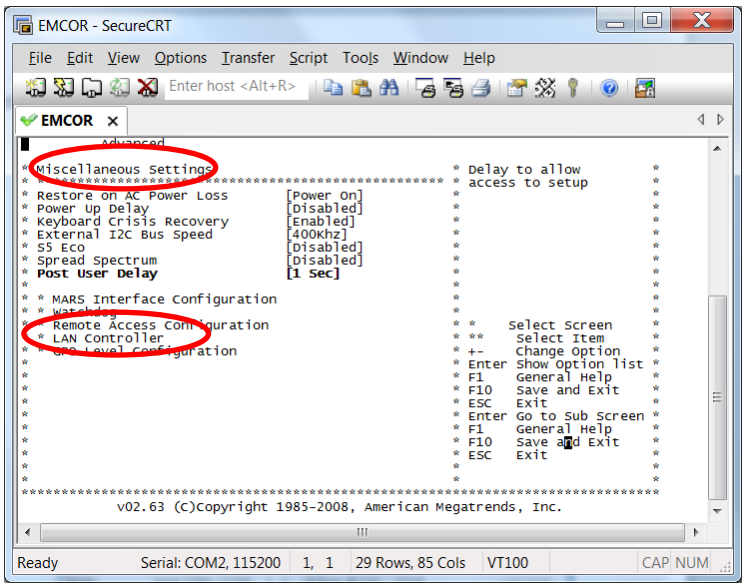


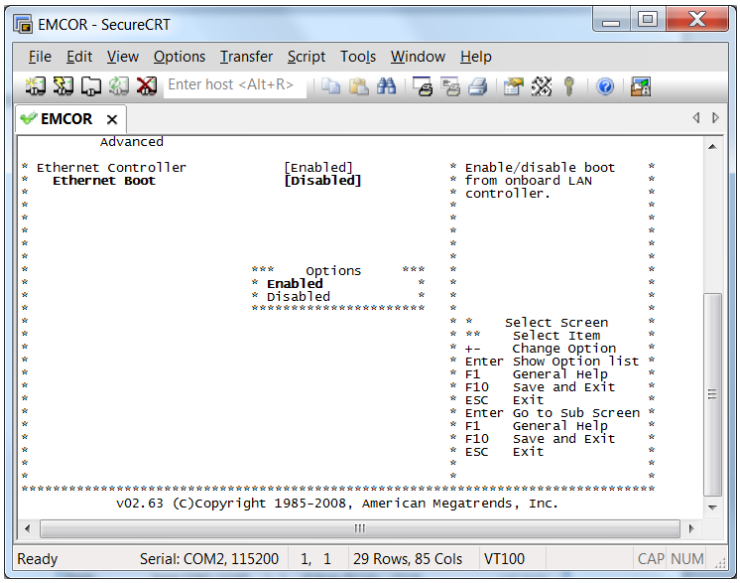


7. While on »Miscellaneous«, select »Post Users Delay«, select »5 seconds« and hit Enter.

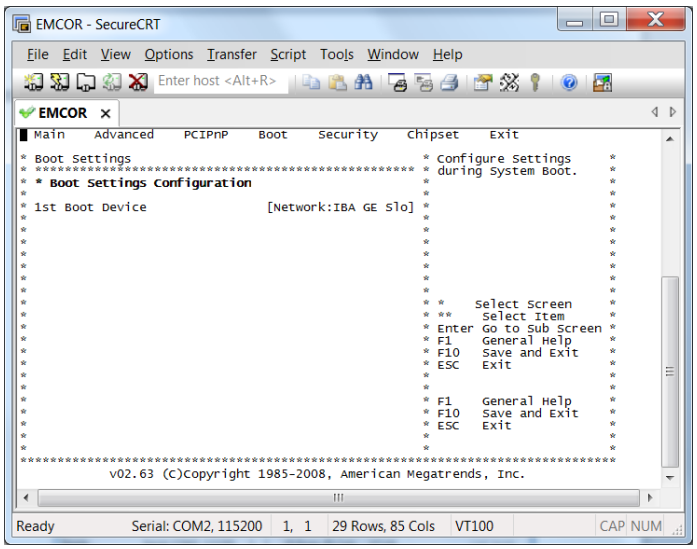


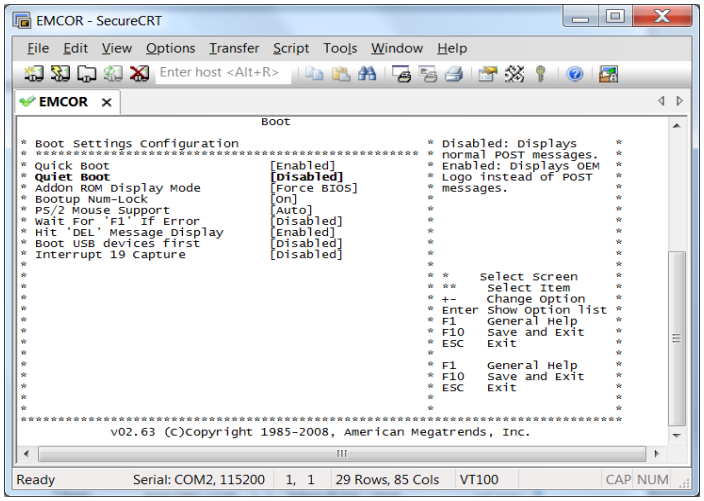
8. While on »Miscellaneous«, scroll down to »Lan Controller« and »Enable« Ethernet Boot.



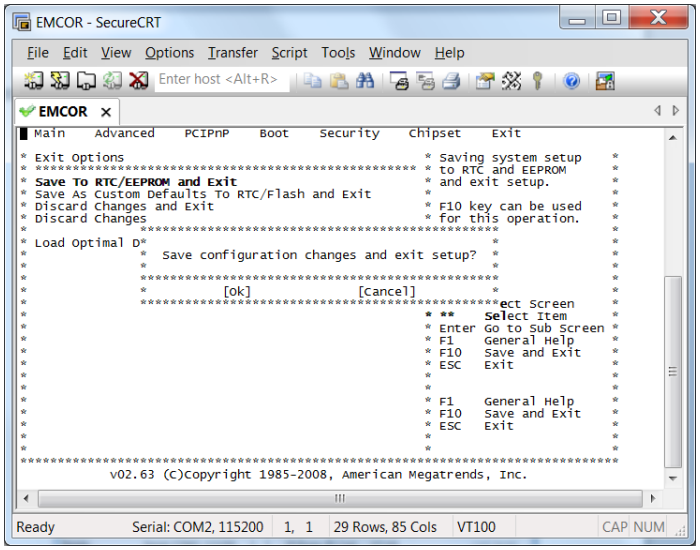


9. Hit »ESC« and use arrow to go to »BOOT« menu . Select »Boot Settings Configuration« and disable »Quiet Boot«.

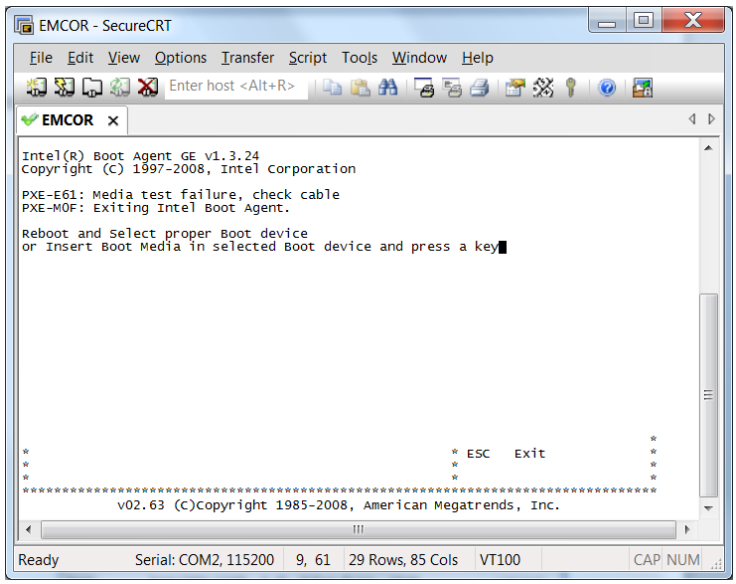




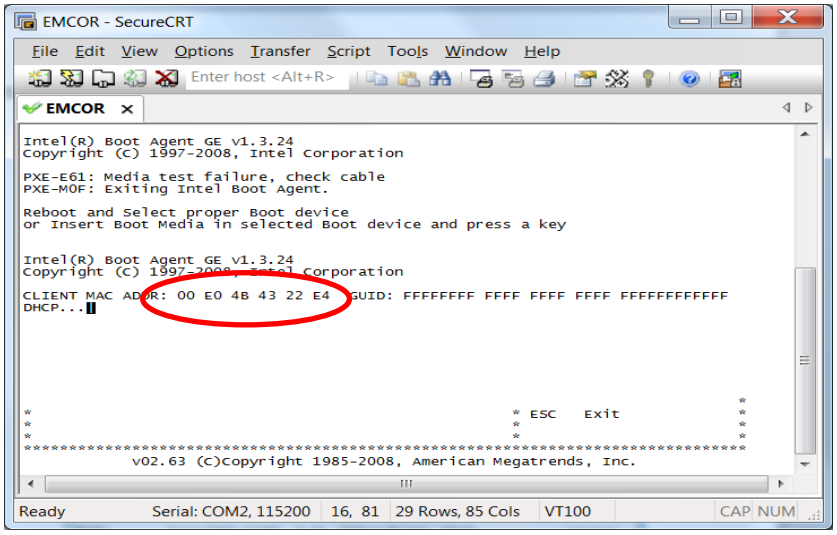
10. Hit »ESC« and use arrow to go to »EXIT« Menu. Hit Enter to »Save to RTC/EEPROM and Exit«. Hit Enter again to confirm »OK« . (F10 save and exit does not work)



11. After exiting BIOS, the terminal will display message »Reboot and Select proper Boot device«. Connect Ethernet cable from Network switch to CA EPICS port on the EMCOR controller.



12. Press any key to restart. The MAC address will apprear on screen as it is trying to contact DHCP server.

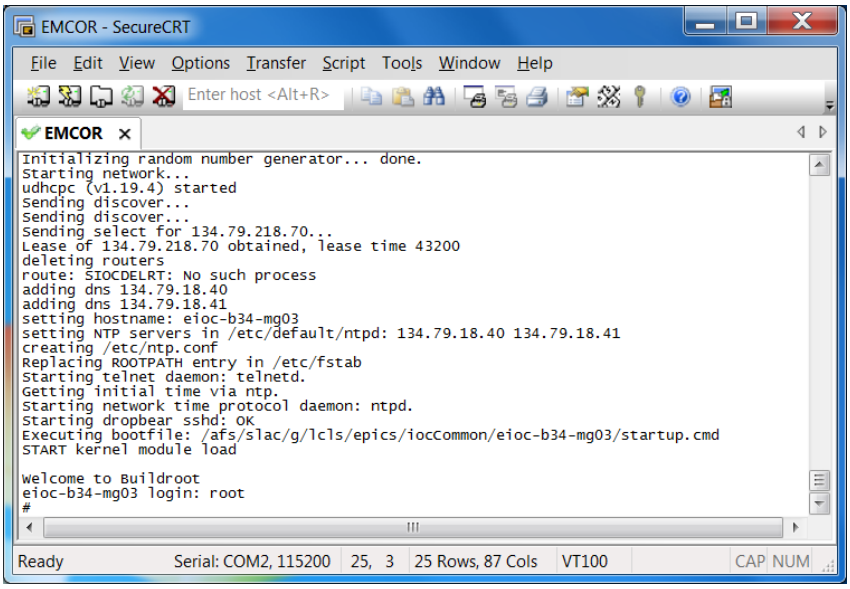


13. Write down MAC address, and put it in the `dhcpd.conf` file located at: /afs/slac/service/dhcp-pxe/dhcpd.conf. (permissions are requireed to change DHCP file. Contact Ernest or Thuy)

14. Check and restart DHCP Server (need permissions):

```
remctl dhcp3 dhcp check
remctl dhcp3 dhcp restart
```

15. After MAC address and node name are defined in DHCP file, power cycle the controller to observe the CPU boot completely and successful with node name entered in DHCP. Example: “eioc-b34-mg03”



Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

4.2. File setup [TC-EMCOR-CP-02]

Setup the files required to boot, load kernel modules for EPICS access and test program

Pre-requisites

1. Procedure 4.1

Test procedure

1. Go to location `$IOC`:

```
cd $IOC
```

2. Directory with the node name of the IOC should be created with the following files inside:
   - README
   - startup.cmd (mount the NFS hard Drive)
   - kernel-modules.cmd (load up driver)
   - startup-epics.cmd (Start EPICS in the background)
   - startupConsole.cmd (Start EPICS in the foreground)
3. Create directory vioc-<NODE ID> (Example: `VIOC-B34-CD41`). It should contain these folders:
   - iocStartup.cmd*
   - screenrc
   - bin@ - create this link

Files can be copied from another IOC that's already setup.

4. At location `/afs/slac/g/lcls/tftpboot/linuxRT/boot/` create boot file in the following form: ioc-b34-cd41.ipxe.
5. On location $IOC_DATA make directories for:
   (a) ioc-b34-cd41: for saving IOC booting messeages.
   (b) vioc-b34-cd41: for saving EPICS IOC messeages.
6. `Create` subdirectory `Autosave, autosave-req, iocInfo under` »vioc-b34-cd41« (Example: `vioc-b34-cd41`).

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

4.3. Connections setup [TC-EMCOR-CP-03]

Setup the »iocConsole« and network connections.

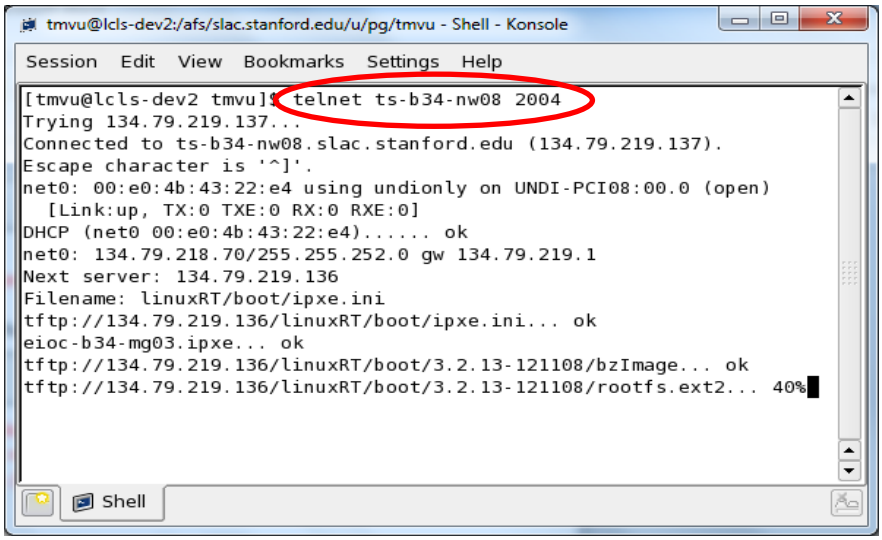
Pre-requisites

1. Procedure 4.2

Test procedure

1. Connect COM port (RS232) from EMCOR controller to available port on DIGI port server TS16 using a straight Ethernet RJ45 to RJ45 cable.

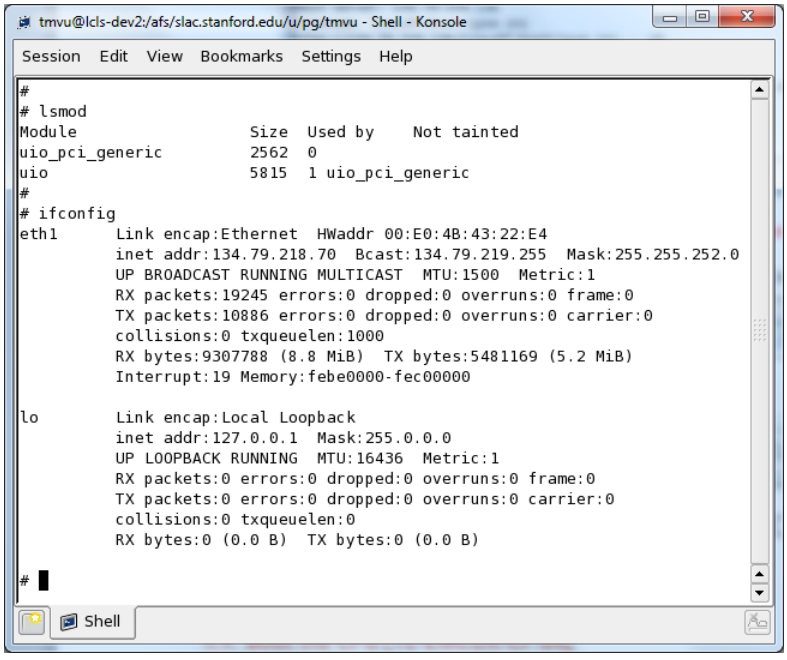
2. Setup DIGI port server by connecting to its web interface https://<DIGI-NODE>. (User ID and password requied. Contact Charlie Granieri). Set port baud rate as 115200, 8N1.
3. Connect to the CPU from any lcls-dev2 terminal using telnet command. Successfull log in confirms the Digi port is working. To exit telnet session, hit ctl A] and type quit.
   Port 1 is 2001
   telnet <digi name> <port>



4. To use iocConsole, add IOC name, DIGI name and port to `screeniocs` file (Location $IOC).
5. Commit it to version control: (»notes« is text that describe changes in screenioc file)

```
cvs commit -m  »notes« screeniocs
```

6. Assuming the network cable is connected from previous setup to Ethernet eth0 (CA EPICS), from any lcls-dev2 terminal, type: iocConsole »IOC node name«. If successful, you can type some commands and see the output return. (Ex: ifconfig, lspci, lsmode, etc.)



Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

4.4. **Boot the CPU [TC-EMCOR-CP-04]**

Start the CPU.

Pre-requisites

1. Procedure 4.3

Test procedure

1. Start the CPU by connecting it to the power supply.
2. Connect to the board with the `iocConsole` command and check that the booting sequence can be observed.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

4.5. **Activate Fast Feedback network chip [TC-EMCOR-CP-05]**

Setup fast feedback network chip.

Pre-requisites

1. Procedure 4.4

Test procedure (with brand new EMCOR controller)

1. Obtain PCI signature (domain/bus/dev/fun) of target device. Command should display two Ethernet controllers: 08:00.0 and 07:00.0.

```
lspci | grep Ethernet
```

2. Check which network is online, connected to Channel Access.

```
ifconfig -a | grep eth
```

3. Discover which PCI signature for Channel Access (00:08.0) and the other signature (00:07.0) should be for the second NIC (Fast Feedback).

```
ethtool -i eth0
```

4. Become root.
5. Change directory to location of the program and the FLASH.eep image.

```
cd /afs/slac/package/linuxRT/tools/e1k-nvm
```

6. Make sure e1k driver is not bound. (Will not be the case if the flash is blank if it is a brand new EMCOR Controller). Unbind the device:


```
echo 0000:07:00.0 > /sys/bus/pci/drivers/e1000e/unbind
```

7. Execute writting MAC address and verify. (MAC address and image can be written at the same time or separately). Verify passed with no errors.

```
./e1k-nvm –s 07:00.0 –M <Mac address> -i ./82574_NO_MNG_A1_NoL0s_FLASH.eep -wV
```

8. Confirm the new SLAC MAC Address was written:

```
./e1k-nvm –m -s 07:00.0
```

9. Power cycle and it will automactically bind the device that has the flashed MAC. Confirm by observing two network configs:

```
ifconfig –a |grep eth
```

10. Note: To change the MAC Address that already has the image, execute:

```
./e1k-nvm –M <Mac address> -s 07:00.0
```

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

1. Label [TC-EMCOR-CP-06]

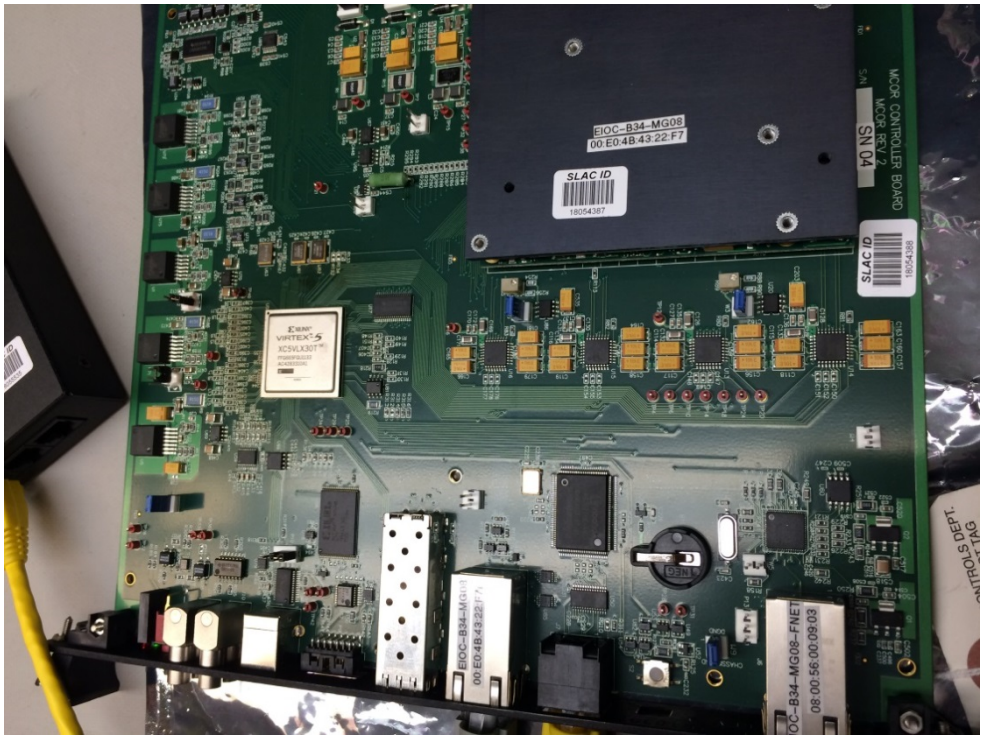
Label the board.

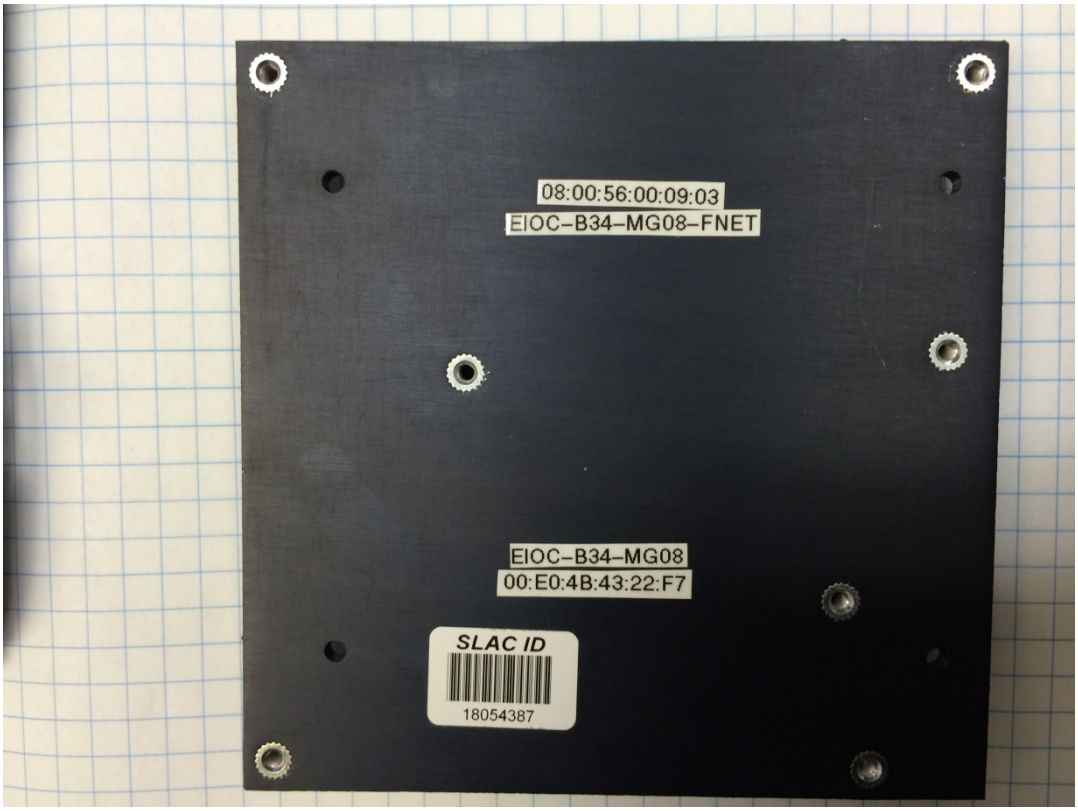
Pre-requisites

1. Procedure 4.5

Test procedure

1. Label and Depot Slac ID and MAC address.





Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

5. Automated Tests

This chapter describes the details of each of the automated tests. Before they are run, these procedures should be performed:

- All CPU/OS procedures.
- Connect to the EMCOR controller, stop all EPICS applications. (Check if EPICS is running by issuing command: »screen –ls« . Output should be No Sockets found)
- Start the program that exposes EMCOR Controller PCI registers on the network:

```
/afs/slac/g/lcls/package/remote-pci-register-access/rio-server/build-
linuxRT/src/rios 0000:01:00.0@0
```

- Install EMCOR testing software (see Appendix A).
- Appropriate configuration for the tests needs to be set by editing testconf.ini file in the EMCOR-Tests module. Mainly `IP_CONTROLLER`, `IP_TESTER`, `FULLSCALE_ADC_MON`, `FULLSCALE_ADC_FDBCK` and `FULLSCALE_DAC` values should be set accordingly.

To actually run the tests, use emcor_tests_gui.py script. The GUI will be shown in which all of the tests can be chosen and run separately. It is recommended to just select "All tests" label and click on Run button to run all the tests. In the following chapters test procedures for each of the automated tests are described in the details. There is no need to run or perform them separately.

Additional GUI is available for checking if the device is connected and working. It can be started by running emcor_channels_gui.py script.

5.1. Channels AIO test [TC-EMCOR-AU-01]

Analog channels are set to different values which are then read back and compared to the original ones.

Pre-requisites

1. Tester board connected on the back of the controller board.

Test tracking

All tests/test_emcor_aio/AIOTests/test_channels

Test procedure

1. Set values on all analog channels to 0.
2. Set value on one analog channel to the maximum value.
3. Read back the value and make a comparison with the set value. Check that the difference between the values is lower than the defined maximum difference.
4. Read back values from other analog channels as well and check that they are 0.

5. Repeat the whole procedure until all the channels have been tested.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

5.2. Linearity [TC-EMCOR-AU-02]

Analog channels are set to different values which are then read back and compared to the original ones.

Pre-requisites

1. Tester board connected on the back of the controller board.

Test tracking

All tests/test_emcor_aio/AIOTests/test_linearity

Test procedure

1. Set value on one analog channel to the minimum value.
2. Read back the value and make a comparison with the set value. Check that the difference between the values is lower than the defined maximum difference of 0.1%.
3. Repeat steps 1 and 2 for the same channel now using value that is 0.5 units bigger. Repeat until the tested value reaches maximum value.
4. Repeat the whole procedure until all the channels have been tested.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

5.3. Linear ramping [TC-EMCOR-AU-03]

Linear ramping is enabled and a value is set on the channel, which is then continuously read and the value checked.

Pre-requisites

1. Tester board connected on the back of the controller board.

Test tracking

All tests/test_emcor_aio/AIOTimingTests/test_linear_ramping

Test procedure

1. Set value on one analog channel to zero.

2. Enable ramping on the channel and set the ramping rate in such a way that maximum value is reached after 1 second.
3. Set value on the channel to the maximum value.
4. Continuously read back the value and check if it is rising linearly.
5. Repeat the whole procedure until all the channels have been tested.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

5.4. DAC output on fault [TC-EMCOR-AU-04]

When analog channel faults, its DAC output should be set to 0.

Pre-requisites

1. Tester board connected on the back of the controller board.

Test tracking

All tests/test_emcor_aio/FunctionalTests/test_fault_output

Test procedure

1. Set value on one analog channel to its maximum value.
2. Set EMCOR fault bit for this channel on the tester board.
3. Read the monitor/feedback value for the channel and check that it is 0.
4. Repeat the whole procedure until all the channels have been tested.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

5.5. ADC timeouts test [TC-EMCOR-AU-05]

ADC timeouts data is read from FPGA and checked that it is valid.

Pre-requisites

Test tracking

All tests/test_emcor_basic/ADCTimeoutTests/test_adc_timeout

All tests/test_emcor_basic/ADCTimeoutTests/test_bulk_adc_timeout

Test procedure

1. Read ADC timeouts data.
2. Check that the EMCOR ADC and bulk ADC timeout bits are not set.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

5.6. System info test [TC-EMCOR-AU-06]

System information is read from the FPGA and checked if it is valid.

Pre-requisites

Test tracking

All tests/test_emcor_basic/SystemInfoTests/test_firmware_date

All tests/test_emcor_basic/SystemInfoTests/test_firmware_version

All tests/test_emcor_basic/SystemInfoTests/test_sub_type

All tests/test_emcor_basic/SystemInfoTests/test_system_id

Test procedure

1. Read controller board system information.
2. Firmware version should be 8.51.
3. Firmware date should be 01/15/2015.
4. System ID should be "MCOR" and subsystem ID should be "REV02".

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

5.7. Voltage monitor test [TC-EMCOR-AU-07]

Data about board voltages is read from the FPGA and checked if it is valid.

Pre-requisites

Test tracking

All tests/test_emcor_basic/VoltageMonitorTests/test_temperature

All tests/test_emcor_basic/VoltageMonitorTests/test_voltage_12

All tests/test_emcor_basic/VoltageMonitorTests/test_voltage_15

All tests/test_emcor_basic/VoltageMonitorTests/test_voltage_33

All tests/test_emcor_basic/VoltageMonitorTests/test_voltage_33io

All tests/test_emcor_basic/VoltageMonitorTests/test_voltage_5

All tests/test_emcor_basic/VoltageMonitorTests/test_voltage_m15

Test procedure

1. Read voltage monitor data.
2. All the voltages should be within +/- 5% of their nominal values. Temperature value should be between 60°F and 100°F.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

5.8. **Xilinx system monitor test [TC-EMCOR-AU-08]**

Xilinx system monitor data is read from the FPGA and checked if it is valid.

Pre-requisites

Test tracking

All tests/test_emcor_basic/XilinxSystemMonitorTests/test_temp_cur

All tests/test_emcor_basic/XilinxSystemMonitorTests/test_temp_max

All tests/test_emcor_basic/XilinxSystemMonitorTests/test_temp_min

All tests/test_emcor_basic/XilinxSystemMonitorTests/test_vaux_cur

All tests/test_emcor_basic/XilinxSystemMonitorTests/test_vint_cur

Test procedure

1. Read Xilinx system monitor data.
2. All the voltage values should be within +/- 5% of their nominal values. Temperature value should be between 80°F and 150°F.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

5.9. **EMCOR faults DI test [TC-EMCOR-AU-09]**

EMCOR fault bits are set on the tester board and read on the controller board.

Pre-requisites

1. Tester board connected on the back of the controller board.

Test tracking

All tests/test_emcor_dio/DITests/test_emcor_faults

Test procedure

1. Clear all EMCOR fault bits on the tester board.
2. Set one EMCOR fault bit on the tester board to 1.
3. Read EMCOR fault bits on the controller board and check that the right one is set and the others are cleared.
4. Also check and store the information if the bit is stuck high or low by performing AND and OR operations between read register and temporary values.
5. Repeat the whole procedure until all the EMCOR fault bits have been tested.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

5.10. **Magnet faults DI test [TC-EMCOR-AU-10]**

Magnet fault bits are set on the tester board and read on the controller board.

Pre-requisites

1. Tester board connected on the back of the controller board.

Test tracking

All tests/test_emcor_dio/DITests/test_magnet_faults

Test procedure

1. Clear all magnet fault bits on the tester board.
2. Set one magnet fault bit on the tester board to 1.
3. Read magnet fault bits on the controller board and check that the right one is set and the others are cleared.
4. Also check and store the information if the bit is stuck high or low by performing AND and OR operations between read register and temporary values.
5. Repeat the whole procedure until all the magnet fault bits have been tested.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

5.11. Control DO tests [TC-EMCOR-AU-11]

Control bits are set on the controller board and read on the tester board.

Pre-requisites

1. Tester board connected on the back of the controller board.

Test tracking

All tests/test_emcor_dio/DOTests/test_inhibit_bit

All tests/test_emcor_dio/DOTests/test_reset_bit

Test procedure

1. Clear Reset bit on the controller board.
2. Set Reset bit on the controller board.
3. Read Reset bit on the tester board and check that it is set.
4. Clear Reset bit on the controller board.
5. Read Reset bit on the tester board and check that it is cleared.
6. Repeat the whole procedure also for Inhibit bit.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

5.12. Interlocks DO test [TC-EMCOR-AU-12]

Interlocks are set on the controller board and read on the tester board.

Pre-requisites

1. Tester board connected on the back of the controller board.

Test tracking

All tests/test_emcor_dio/DOTests/test_interlocks

Test procedure

1. Clear all interlocks on the controller board.
2. Set one interlock on the controller board to 1.
3. Read interlock bits on the tester board and check that the right one is set and the others are cleared.
4. Also check and store the information if the bit is stuck high or low by performing AND and OR operations between read register and temporary values.
5. Repeat the whole procedure until all the interlock bits have been tested.

Test result: ☐ Not tested ☐ Passed ☐ Passed with reservations ☐ Failed

Comment:

Appendix A. Installation of EMCOR testing software

For testing EMCOR board, special software modules were written that are able to talk with the EMCOR controller and tester over the network and perform some tests and show their results in a GUI. Installation procedure:

1. Install Python 2.7 on your machine. On windows, you need path to Python interpreter in your PATH variable. This is usually done automatically on installation.
2. Install PyQT 4 (4.11.3). It can be obtained from this webpage. Appropriate version must be downloaded and installed that matches installed Python version (32/64 bit).
3. Obtain utility Python modules from the SLAC CVS:

   ```
   eco -m Python-RemotePCI
   eco -m Python-UnitTestGUI
   ```

   Module descriptions:
   - Python-RemotePCI - Communication library for talking with the server that exposes device registers on the network.
   - Python-UnitTestGUI - GUI library for running Python unit tests.
4. Obtain sources for EMCOR testing software from the SLAC CVS. On Linux you can do that with special ***eco*** tool:

   ```
   eco -m emcorTester
   ```

   There are three source modules:
   - EMCOR-Controller - Library for communicating with EMCOR controller board.
   - EMCOR-Tester - Library for communicating with EMCOR tester board.
   - EMCOR-Tests - Core module that uses all the others and contains all the tests and GUIs for testing EMCOR controller board.
5. Before core module can be used, all the utility and library modules need to be installed. This can be done by going into their folders and running this command in the command line:

   ```
   python setup.py install
   ```

6. After that EMCOR-Tests module will be ready to be used.