CHAPTER FIVE: *Check Waveform Status*

In this chapter, see how

- ***To use status registers***

Use Status Registers

A wide range of status registers allows you to quickly determine Waverunner internal processing status at any time. These registers and the oscilloscope's status reporting system, which group related functions together, are designed to comply with IEEE 488.2 recommendations. Some, such as the Status Byte Register (STB) or the Standard Event Status Register (ESR), are required by the IEEE 488.2 Standard. Others are device specific, including the Command Error Register (CMR) and Execution Error Register (EXR). Those commands associated with IEEE 488.2 mandatory status registers are preceded by an asterisk (*).

OVERVIEW

The Standard Event Status Bit (ESB) and the Internal Status Change Bit (INB) in the SBR are summary bits of the ESR and the Internal State Change Register (INR). The Message Available Bit (MAV) is set whenever there are data bytes in the output queue. The Value Adapted Bit (VAB) indicates that a parameter value was adapted during a previous command interpretation. For example, if the command TDIV 2.5 US was received, the timebase would be set to 2 ms/div along with the VAB bit.

The Master Summary Status bit (MSS) indicates a request for service from the oscilloscope. You can only set the MSS bit if you have enabled one or more of the other STB bits with the Service Request Enable Register (SRE).

All Enable registers (SRE, ESE and INE) are used to generate a bit-wise AND with their associated status registers. The logical OR of this operation is reported to the STB register. At power-on, all Enable registers are zero, inhibiting any reporting to the STB.

The ESR primarily summarizes errors, whereas the INR reports internal changes to the instrument. Additional details of errors reported by ESR can be obtained with the queries `CMR?`, `DDR?`, `EXR?` and `URR?`.

The register structure contains one additional register, not shown on the next page (Fig.1). This is the Parallel Poll Enable Register (PRE), which behaves exactly like the SRE, but sets the "ist" bit used in the Parallel Poll. Read the "ist" bit with the `*IST?` query.

Example: If you were to send the erroneous command TRIG_MAKE SINGLE to your Waverunner, the oscilloscope would reject it and set the Command Error Register (CMR) to the value 1 (unrecognized command/query header). The non-zero value of CMR would be reported to Bit 5 of the Standard Event Status Register (ESR), which is then set. Nothing further would occur unless the corresponding Bit 5 of the Standard Event Status Enable Register (ESE) was set with the command `*ESE 32`, enabling Bit 5 of ESR to be set for reporting to the summary bit ESB of the STB.

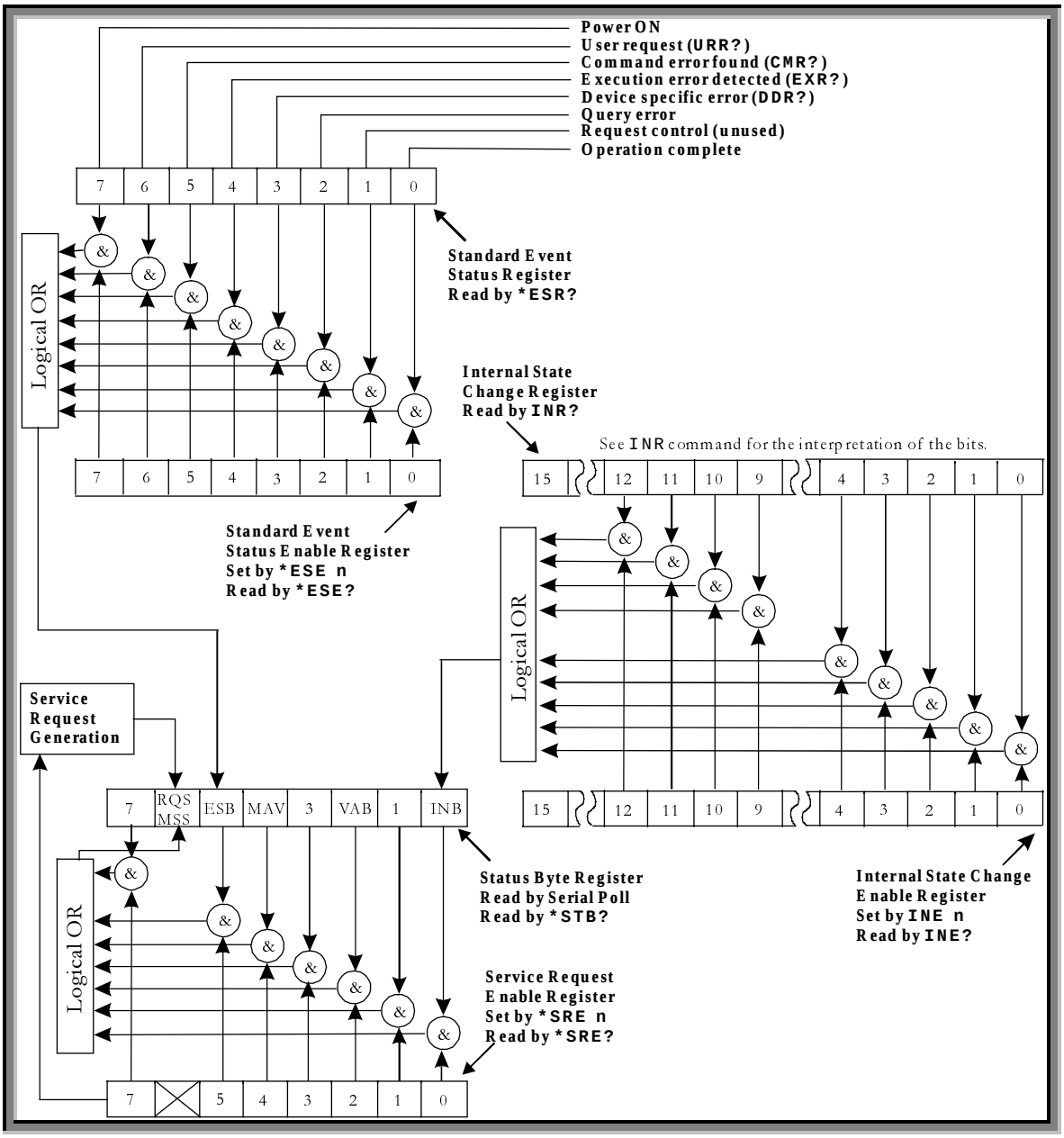

Figure 1.Status Register Structure

If you enabled the setting of the ESB summary bit in STB, again nothing would occur unless you enabled further reporting by setting the corresponding bit in the Service Request Enable Register with the command `*SRE 32`. The generation of a non-zero value of CMR would ripple through to MSS, generating a Service Request (SRQ).

You can read the value of CMR and simultaneously reset to zero at any time with the command `CMR?`. The occurrence of a command error can also be detected by analyzing the response to `*ESR?`. However, if you must survey several types of potential errors, it is usually far more efficient to enable propagation of the errors of interest into the STB with the enable registers ESE and INE.

To summarize: a command error (CMR) sets Bit 5 of ESR if

a. Bit 5 of ESE is set, ESB of STB is also set, or

b. Bit 5 of SRE is set, MSS/RQS of STB is also set and a Service Request is generated.

STATUS BYTE REGISTER (STB)

STB is the Waverunner central reporting structure. It is made up of eight single-bit summary messages, three of which are unused, that reflect the current status of the oscilloscope's associated data structures:

- Bit 0 is the INB summary bit of the Internal State Change Register. It is set if any INR bits are set, provided they are enabled by the corresponding bit of the INE register.
- Bit 2 is the VAB bit, indicating that a parameter value was adapted during a previous command interpretation.
- Bit 4 is the MAV bit, indicating that the interface output queue is not empty.
- Bit 5 is the summary bit ESB of the ESR. It is set if any of the bits of the ESR are set, provided they are enabled by the corresponding bit of the ESE register.
- Bit 6 is either the MSS or RQS (Request for Service) bit.

You can read the STB using the `*STB?` query. It reads and clears the STB, in which case Bit 6 is the MSS bit, And it indicates whether the oscilloscope has any reason to request service. The response to the query represents the binary weighted sum of the register bits. The register is cleared by `*STB?`, `ALST?`, `*CLS`, or with Waverunner powering up.

Another way to read the STB is using the serial poll (see Chapter 2). In this case, Bit 6 is the RQS bit, indicating that the instrument has activated the SRQ line on the GPIB. The serial poll clears only the RQS bit. And the STB's MSS bit, and any other bits which caused MSS to be set, will remain set after the poll. These bits must be reset.

STANDARD EVENT STATUS REGISTER (ESR)

ESR is a 16-bit register reflecting the occurrence of events. ESR bit assignments have been standardized by IEEE 488.2. Only the lower eight bits are currently in use.

Read ESR using *ESR?. The response is the binary weighted sum of the register bits. The register is cleared with *ESR? or ALST?, or with *CLS or powering on the scope.

Example: The response message *ESR 160 tells you that a command error occurred and that the ESR is being read for the first time after power-on. The value 160 can be broken down into 128 (Bit 7) plus 32 (bit 5). See the table with the ESR command description in Part Two for the conditions corresponding to the bits set.

The Power ON bit appears only on the first *ESR? query after power-on, as the query clears the register. You can determine this type of command error by reading the CMR with CMR?. It is not necessary that you read, or simultaneously clear, this register in order to set the CMR bit in the ESR on the next command error.

STANDARD EVENT STATUS ENABLE REGISTER (ESE)

This register allows you to report one or more events in the ESR to the ESB summary bit in the STB.

Modify ESE with *ESE and clear it with *ESE 0, or with power-on. Read it with *ESE?.

Example: Use *ESE 4 to set bit 2 (binary 4) of the ESE Register, and enable query errors to be reported.

SERVICE REQUEST ENABLE REGISTER (SRE)

SRE specifies which Status Byte Register summary bit or bits will bring about a service request. This register consists of eight bits. Setting a bit allows the summary bit located at the same bit position in the SBR to generate a service request, provided that the associated event becomes true. Bit 6 (MSS) cannot be set and is always reported as zero in response to *SRE?.

Modify SRE with *SRE and clear it with *SRE 0, or with power-on. Read it using *SRE?.

PARALLEL POLL ENABLE REGISTER (PRE)

This specifies which Status Byte Register summary bit or bits will set the "ist" individual local message. PRE is similar to SRE, but is used to set the parallel poll "ist" bit rather than MSS.

The value of the "ist" may also be read without a Parallel Poll via the query *IST?. The response indicates whether or not the "ist" message has been set (values are 1 or 0).

Modify PRE *PRE and clear it with *PRE 0, or with power-on. Read this register with *PRE?.

Example: Use *PRE 5 to set the register's bits 2 and 0 (decimal 4 and 1).

INTERNAL STATE CHANGE STATUS REGISTER (INR)

INR reports the completion of a number of internal operations (the events tracked by this 16-bit-wide register are listed with the INR? description in Part Two).

Read the register using INR?. The response is the binary weighted sum of the register bits. Clear the register with INR? or ALST?, a *CLS command, or with power-on.

INTERNAL STATE CHANGE ENABLE REGISTER (INE)

INE allows one or more events in the Internal State Change Status Register to be reported to the INB summary bit in the STB.

Modify INE with `INE` and clear it with `INE 0`, or after power-on. Read it with `INE?`.

COMMAND ERROR STATUS REGISTER (CMR)

This register contains the code of the last command error detected by the oscilloscope. List these error codes using `CMR?`.

Read CMR with `CMR?`. The response is the error code. Clear the register with a `CMR?` or `ALST?` query, a `*CLS` command, or with power-on.

DEVICE DEPENDENT ERROR STATUS REGISTER (DDR)

DDR indicates the type of hardware errors affecting your Waverunner. Individual bits in this register report specific hardware failures. List them using `DDR?`.

Also read this register using the `DDR?` query. The response is the binary weighted sum of the error bits. Clear it with another `DDR?` or with `ALST?`, a `*CLS` command, or with power-on.

EXECUTION ERROR STATUS REGISTER (EXR)

EXR contains the code of the last execution error detected by the oscilloscope. List these error codes with `EXR?`.

Read the register, again using the `EXR?` query. The response is the error code. Clear with another `EXR?` or with `ALST?`, a `*CLS` command, or with power-on.

USER REQUEST STATUS REGISTER (URR)

Finally, URR contains the identification code of the last menu button pressed. List these codes with `URR?`.

Read URR using the same query. The response is the decimal code associated with the selected menu button. And clear the register with another `URR?`, or with `ALST?`, a *CLS command, or with power-on.

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